

T-75-07-15

# UM93520A/B

## Speech Recording and Reproduction IC (with DRAM)

PRELIMINARY

### Features:

- Uses ADM algorithm to process voice data
- Built-in DRAM refresh circuit
- Three selectable sampling rates:
  - UM93520A with one 256K DRAM: 16 KHz or 22 KHz by pin option
  - UM93520B with two 256K DRAMs: 32 KHz
- On-chip oscillator for 3.579545 MHz crystal oscillator
- Single 5-volt power supply
- Available in 28 pin DIP (UM93520A/B) or 48-pin flat package (UM93520AF/BF)

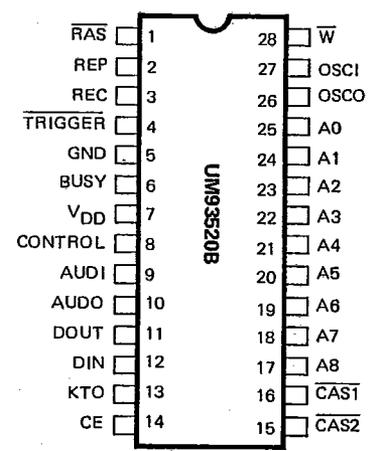
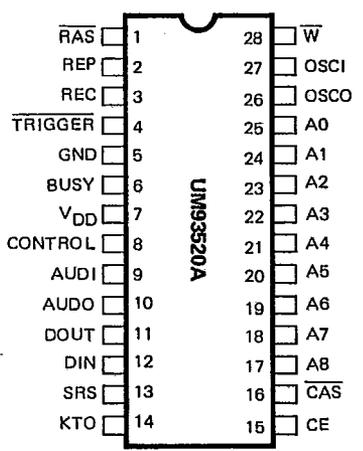
### General Description

The UM93520A/B is a single-chip CMOS LSI for voice recording and reproducing. This chip is especially suitable for use as the recording and playback element of an answering machine. The design of this chip is based on Adaptive Delta Modulation (ADM) technology. Voice

data is recorded and stored on 256K DRAMs. Each 256K DRAM can store 16 seconds of voice data at 16KHz sampling rate, 11.2 seconds at 22KHz sampling rate and 8 seconds at 32KHz sampling rate.

### Pin Configurations

#### 1. 28-pin DIP

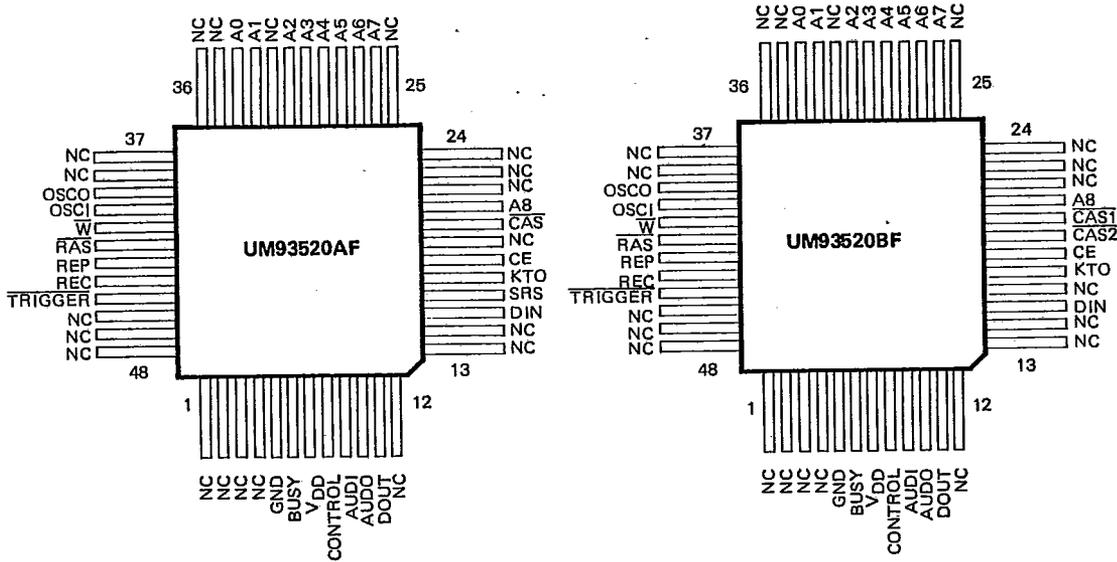




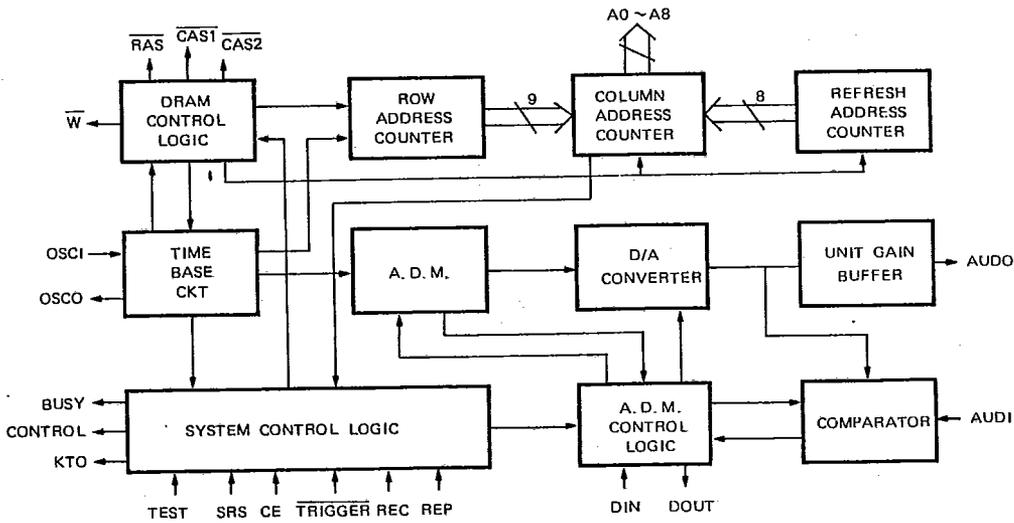
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2. 48-pin flat package



Block Diagram



Telephone Related Products



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Pin Description

| Pin No.                 |                         | Symbol                      | I/O | Description  |
|-------------------------|-------------------------|-----------------------------|-----|--|
| UM93520A<br>(UM93520AF) | UM93520B<br>(UM93520BF) |                             |     |  |
| 1 (42)                  | 1 (42)                  | $\overline{\text{RAS}}$     | O   | Row address strobe output pin. Connected to the $\overline{\text{RAS}}$ pin of the external DRAMs.   |
| 2 (43)                  | 2 (43)                  | REP                         | I   | Reproduction trigger Input pin. Note: RECORD and REP inputs are debounced internally. The debouncing time is typically 300 ms. It's internally pulled low. High activated. |
| 3 (44)                  | 3 (44)                  | REC                         | I   | Recording trigger input pin. It's internally pulled low. High activated.   |
| 4 (45)                  | 4 (45)                  | $\overline{\text{TRIGGER}}$ | I   | Accepts a ring signal of 10.75 sec. duration and enables the chip if no one answers the phone. It's low activated, and internally pulled high.                             |
| 5 (5)                   | 5 (5)                   | GND                         |     | Ground pin.  |
| 6 (6)                   | 6 (6)                   | BUSY                        | O   | Recording/Reproduction state indication output pin. This output will stay high during the recording/reproduction state.  |
| 7 (7)                   | 7 (7)                   | $V_{DD}$                    |     | Power supply +5V. (typ.)   |
| 8 (8)                   | 8 (8)                   | CONTROL                     | O   | Control output pin for tape recorder, high activated.  |
| 9 (9)                   | 9 (9)                   | AUDI                        | I   | Voice input pin for the recorded analog signal.  |
| 10 (10)                 | 10 (10)                 | AUDO                        | O   | Synthesized voice output pin.  |
| 11 (11)                 | 11 (11)                 | DOUT                        | O   | Data output pin. Connected to data input pin of the external DRAMs.  |
| 12 (15)                 | 12 (15)                 | DIN                         | I   | Data input pin. Connected to data output pin of the external DRAMs.  |
| 13 (16)                 |                         | SRS                         | I   | Sample rate select input pin. Connected high, sampling rate is 16 KHz. Connected low, sampling is 22 KHz.  |
| 14 (17)                 | 13 (16)                 | KTO                         | O   | Keytone output pin. The KTO pin is used for keytone output.<br>If SRS is high, keytone is 500 Hz.<br>If SRS is low, keytone is 699 Hz.                                     |
| 15 (18)                 | 14 (18)                 | CE                          | I   | Chip enable pin. High activated. It's internally pulled high. When pulled low, it means "reset the chip"   |
| 16 (20)                 |                         | $\overline{\text{CAS}}$     | O   | Column address strobe output pin. Connected to $\overline{\text{CAS}}$ pin of the external DRAM.   |
|                         | 16 (20)                 | $\overline{\text{CAS1}}$    | O   | Column address strobe output pin. Connected to $\overline{\text{CAS}}$ pin of the external DRAM 1.   |
|                         | 15 (19)                 | $\overline{\text{CAS2}}$    | O   | Column address strobe output pin. Connected to $\overline{\text{CAS}}$ pin of the external DRAM 2.   |



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Pin Description (Continued)

| Pin No.                           |                                   | Symbol    | I/O | Description  |
|-----------------------------------|-----------------------------------|-----------|-----|--|
| UM93520A<br>(UM93520AF)           | UM93520B<br>(UM93520BF)           |           |     |  |
| 17 - 25<br>(21, 26-31, 33,<br>34) | 17 - 25<br>(21, 26-31, 33,<br>34) | A8 - A0   | O   | Address outputs pins to DRAMs.   |
| 26 (39)                           | 26 (39)                           | OSCO      |     | These two pins are for 3.579545 MHz crystal oscillator circuit.          |
| 27 (40)                           | 27 (40)                           | OSCI      |     |  |
| 28 (41)                           | 28 (41)                           | $\bar{W}$ | O   | Write pulse output pin. Connects to $\bar{W}$ pin of the external DRAMs. |

Note: Pins 1, 2, 3, 4, 12, 13, 14, 19, 22, 23, 24, 25, 35, 36, 37, 38, 46, 47, and pin 48 of UM93520AF or UM93520BF are NOT CONNECTED pins.

**Absolute Maximum Ratings \***

Supply Voltage ( $V_{DD}$ ) . . . . . -0.3V to 6V  
 Input Voltage ( $V_{IN}$ ) . . . . . -0.3V to  $V_{DD} + 0.3V$   
 Output Voltage ( $V_{OUT}$ ) . . . . . -0.3V to  $V_{DD} + 0.3V$   
 Operating Temperature ( $T_{OP}$ ) . . . . . -40°C to +125°C  
 Storage Temperature ( $T_{STG}$ ) . . . . . -40°C to +125°C

**\*Comments**

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied and exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**DC Electrical Characteristics** ( $V_{DD} = 5V \pm 10\%$ ,  $T_A = 25^\circ C$ ,  $F_{OSC} = 3.579545$  MHz) unless otherwise specified

| Symbol   | Parameter                                | Min. | Typ. | Max. | Unit     | Conditions   |
|----------|--|------|------|------|----------|--|
| $I_{DD}$ | Standby Current                          |      | 0.2  | 1    | mA       | Output unloaded<br>Input not triggered             |
| $I_{OL}$ | Output sink current<br>(Control, Busy)   |      | 9    |      | mA       | $V_{OL} = 0.8V$                                    |
| $I_{OH}$ | Output source current<br>(Control, Busy) |      | 9    |      | mA       | $V_{OH} = 2.4V$<br>Note: This is an absolute value |
| $V_{OA}$ | Audio output amplitude                   |      | 2.2  |      | $V_{PP}$ | $R_L = 1Kohm$                                      |
| $V_{IH}$ | Input Voltage                            | 2.4  |      |      | V        |  |
| $V_{IL}$ |  |      |      | 0.8  |          |  |





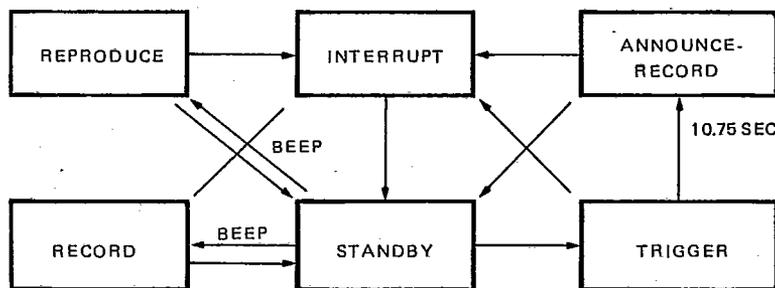
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AC Electrical Characteristics (V<sub>DD</sub> = 5V, T<sub>A</sub> = 25°C, F<sub>OSC</sub> = 3.579545 MHz)

| Symbol            | Parameter                       | Min. | Typ.  | Max. | Unit | Conditions   |
|-------------------|---------------------------------|------|-------|------|------|--|
| t <sub>WR</sub>   | RAS pulse width                 |      | 3.9   |      | μs   | Sampling Rate = 32 KHz                               |
|                   |                                 |      | 3.9   |      |      | Sampling Rate = 16 KHz                               |
|                   |                                 |      | 2.8   |      |      | Sampling Rate = 22 KHz                               |
| t <sub>WC</sub>   | CAS pulse width                 |      | 1.9   |      | μs   | Sampling Rate = 32 KHz                               |
|                   |                                 |      | 1.9   |      |      | Sampling Rate = 16 KHz                               |
|                   |                                 |      | 1.4   |      |      | Sampling Rate = 22 KHz                               |
| t <sub>TRIG</sub> | Trigger Time                    |      | 10.75 |      | sec. | For any sampling Rate                                |
| t <sub>REP</sub>  | Reproduction and recording time |      | 16    |      | sec. | Sampling Rate = 32 KHz                               |
|                   |                                 |      | 16    |      |      | Sampling Rate = 16 KHz                               |
|                   |                                 |      | 11.2  |      |      | Sampling Rate = 22 KHz                               |
| t <sub>TREC</sub> | Tape recording time             |      | 30.75 |      | sec. | For any sampling Rate                                |
| f <sub>KTO</sub>  | KTO frequency recording time    |      | 1000  |      | Hz   | Sampling Rate = 32 KHz                               |
|                   |                                 |      | 500   |      |      | Sampling Rate = 16 KHz                               |
|                   |                                 |      | 699   |      |      | Sampling Rate = 22 KHz                               |
| t <sub>KTO</sub>  | KTO duration time               |      | 0.5   |      | sec. | For any sampling Rate                                |
| t <sub>MINR</sub> | Valid pulse width               | 280  |       |      | ms   | Debouncing time for REC., REP., CE, and TRIGGER pins |

**Functional Description & Timing Diagrams**

1. The operating sequence for recording and reproduction is shown below:



**2. Standby**

The following conditions will cause the chip to enter the standby state:

1. Power on.
2. Completion of operations in the record, reproduce or announce-record states.
3. The cause of an interrupt is cleared.

**3. Recording and reproducing**

Before the announce/recording sequence operates normally, an announcement must have been recorded in advance from within the record state. This can be achieved by pulling the REC pin to high, which will immediately cause a beep to output for 0.5 seconds from the KTO pin.



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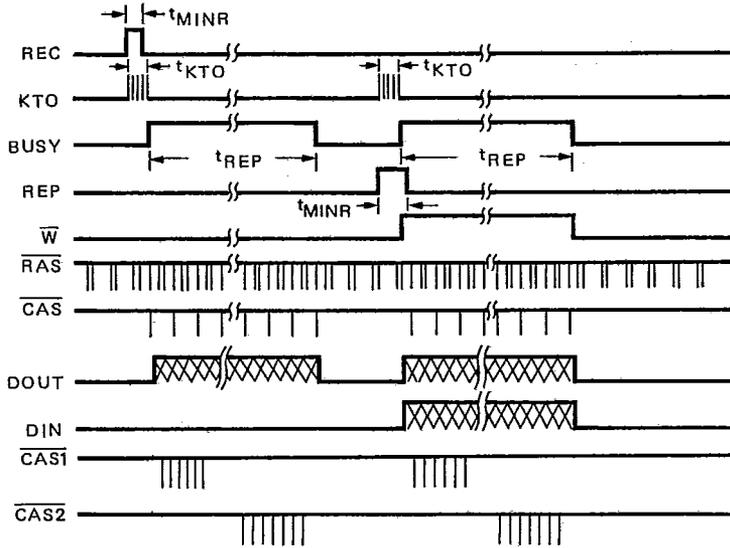
To check an announcement that was recorded previously in the reproduction state, the REP pin can be pulled high and, as in the record state, a beep will be transmitted and the announcement will be sent out from AUDIO.

maximum recording time depend on the sampling frequency, as follows:

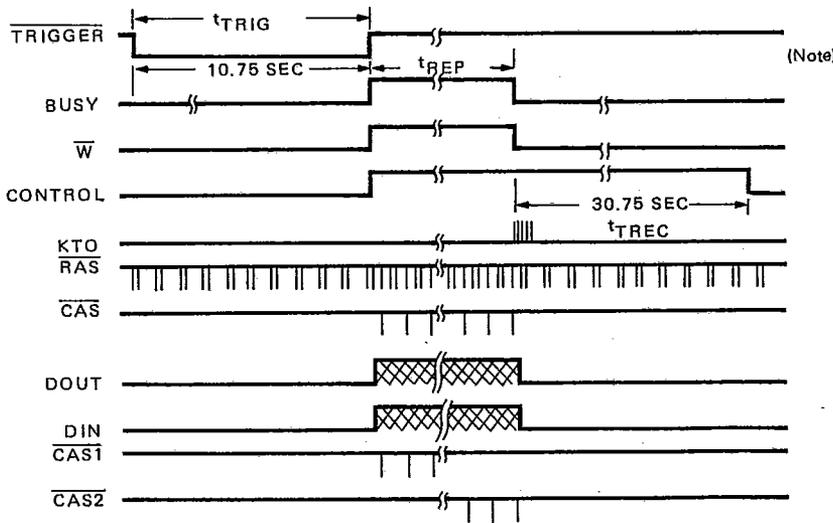
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| Sample Rate        | 16K    | 22K    | 32K   |
|--------------------|--------|--------|-------|
| Beep ( $f_{KTD}$ ) | 500 Hz | 699 Hz | 1 KHz |
| Time ( $t_{REP}$ ) | 16s    | 11.2s  | 16s   |

Both the record and reproduction states can be interrupted by dropping the CE pin to low, which will stop recording or reproduction. The frequency of the beep and the



**4. Announcing and recording**





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**4. Announcing and recording**

The Announce/Record state is triggered when the ring signal from the subscriber loop comes in for more than 10.75 seconds without interruption. In this state, any previously recorded announcement will be sent out, with

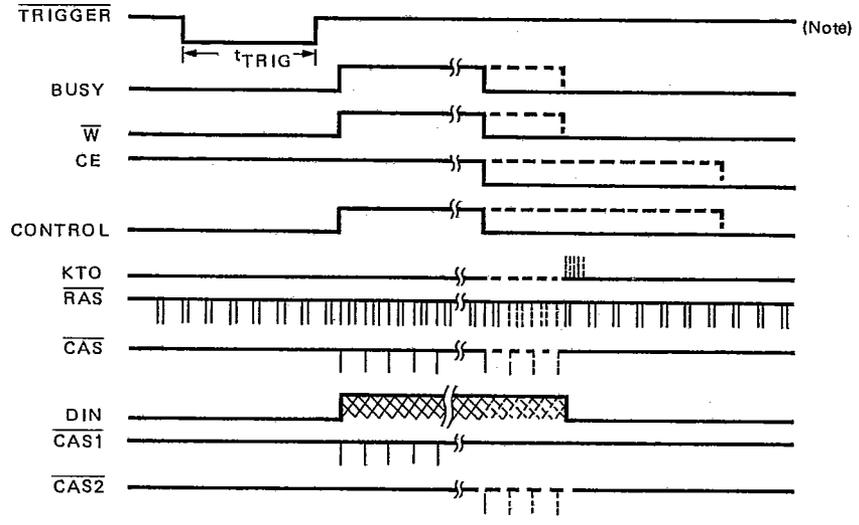
the BUSY and CONTROL pins going high and a tape recorder enabled to record a maximum of 30.75 seconds of voice data. In addition, a beep will be sent out as shown in the diagram below.

**5. Interrupt**

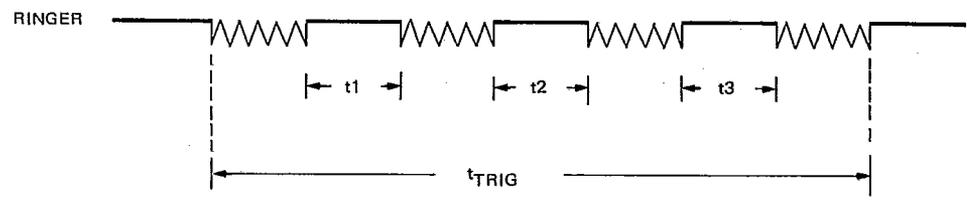
There are two ways to enter the interrupt state:

1. Dropping the CE pin from high to low.
2. The absence of a trigger signal for more than four seconds during the trigger state.

Once a trigger signal is accepted, however, it can no longer be interrupted, even if the caller hooks the telephone handset.



Note: The TRIGGER pin is normally connected to the telephone ringer detector  $t_{TRIG}$  means the time duration after the first signal is on. If pause time between two ringer signals exceeds 4 seconds, the trigger duration will reset to zero. The trigger shown below works, where  $t_{TRIG} \geq 10.75$  seconds and pause time ( $t_1, t_2, t_3$ ) must be less than 4 seconds.



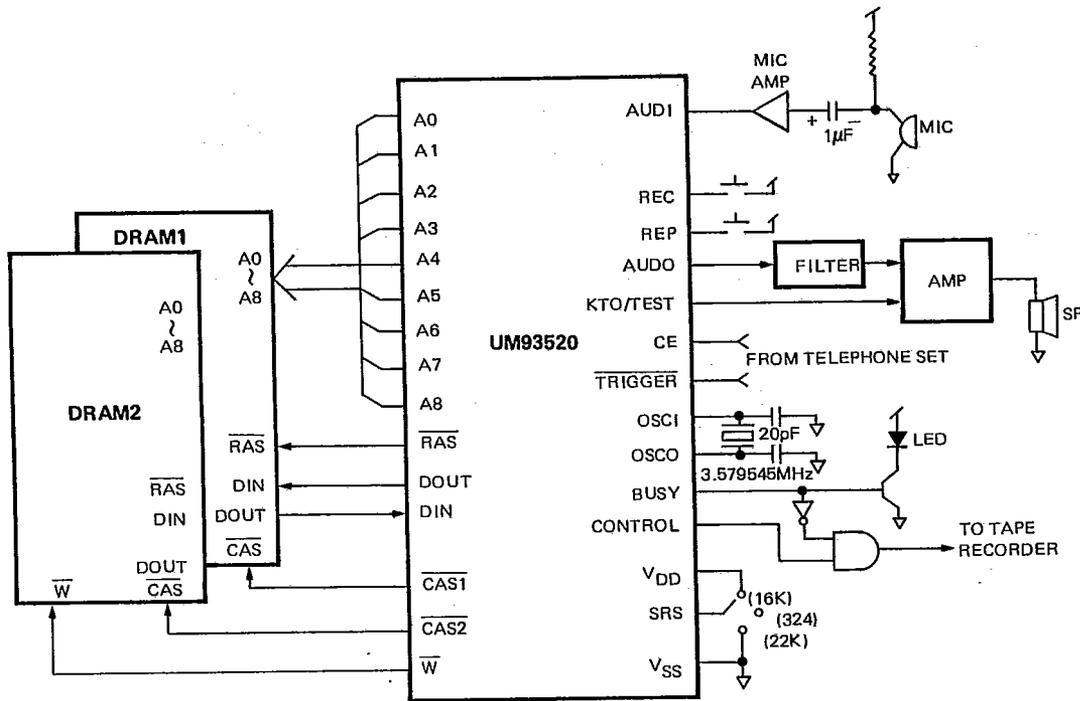


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Applications Circuits

(A) General



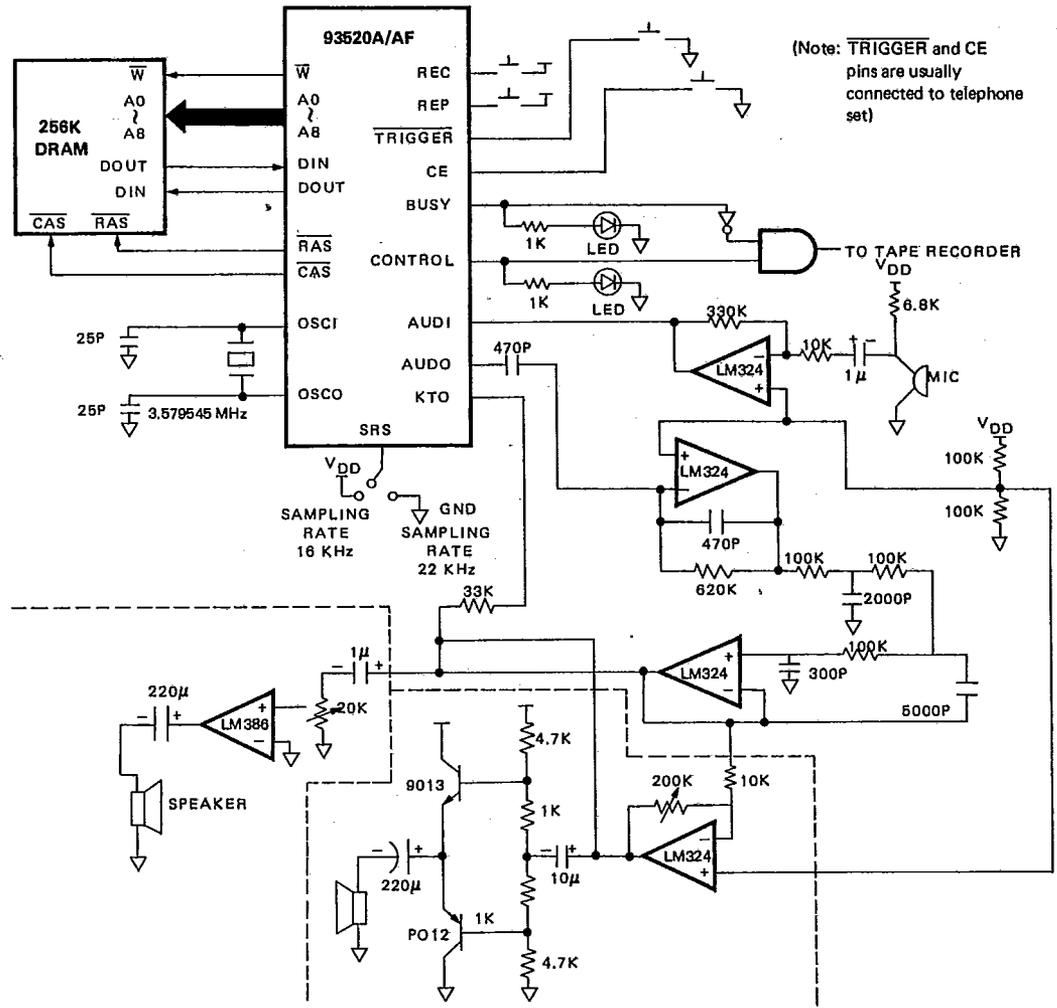


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**Applications Circuits: (Continued)**

(B) UM93520A/UM93520AF







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**Ordering Information**

| Part No.  | Sampling Rate                  | DRAM           | Package |
|-----------|--------------------------------|----------------|---------|
| UM93520A  | 16 KHz or 22 KHz by pin option | one 256K DRAM  | 28L DIP |
| UM93520AF |                                |                | 48L FP  |
| UM93520B  | 32 KHz                         | two 256K DRAMs | 28L DIP |
| UM93520BF |                                |                | 48L FP  |