

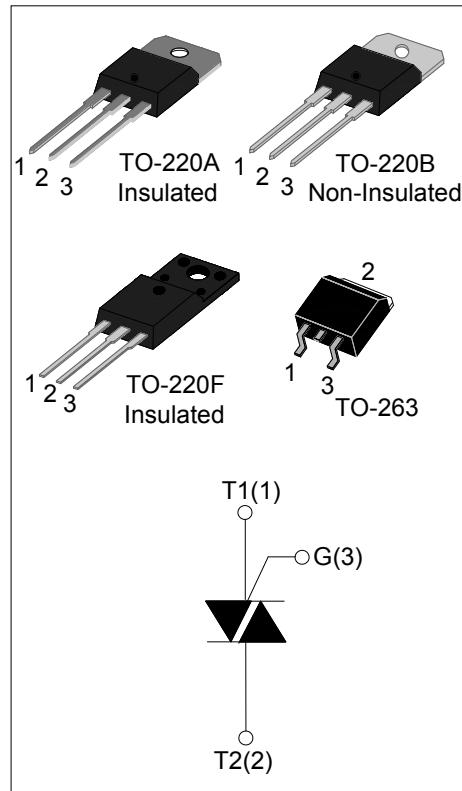


JST16 Series 16A TRIACs

Rev.5.0

DESCRIPTION:

With high ability to withstand the shock loading of large current, JST16 series triacs provide high dv/dt rate with strong resistance to electromagnetic interface. With high commutation performances, 3 quadrants products especially recommended for use on inductive load. From all three terminals to external heatsink, JST16A provides a rated insulation voltage of 2500 V_{RMS}, and JST16F provides a rated insulation voltage of 2000V_{RMS}, complying with UL standards (File ref: E252906).



MAIN FEATURES

Symbol	Value	Unit
I _{T(RMS)}	16	A
V _{DRM} / V _{RRM}	600 and 800 and 1200	V

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Storage junction temperature range	T _{stg}	-40-150	°C
Operating junction temperature range	T _j	-40-125	°C
Repetitive peak off-state voltage (T _j =25°C)	V _{DRM}	600/800/1200	V
Repetitive peak reverse voltage (T _j =25°C)	V _{RRM}	600/800/1200	V
Non repetitive surge peak Off-state voltage	V _{DSM}	V _{DRM} +100	V
Non repetitive peak reverse voltage	V _{RSM}	V _{RRM} +100	V
RMS on-state current	TO-220A(Ins) (T _C =86°C)	16	A
	TO-220B(Non-Ins) (T _C =107°C)		
	TO-220F(Ins) (T _C =90°C)		
	TO-263 (T _C =80°C)		
Non repetitive surge peak on-state current (full cycle, F=50Hz)	I _{TSM}	160	A

I ² t value for fusing (tp=10ms)	I ² t	128	A ² s
Critical rate of rise of on-state current (I _G =2×I _{GT})	dI/dt	50	A/μs
Peak gate current	I _{GM}	4	A
Average gate power dissipation	P _{G(AV)}	1	W
Peak gate power	P _{GM}	5	W

ELECTRICAL CHARACTERISTICS (T_j=25°C unless otherwise specified)

3 Quadrants

Symbol	Test Condition	Quadrant		Value				Unit
				BW	CW	SW	TW	
I _{GT}	V _D =12V R _L =33Ω	I - II -III	MAX	50	35	10	5	mA
V _{GT}		I - II -III	MAX	1.3				V
V _{GD}	V _D =V _{DRM} T _j =125°C R _L =3.3KΩ	I - II -III	MIN	0.2				V
I _L	I _G =1.2I _{GT}	I -III	MAX	70	50	30	15	mA
		II		80	60	40	20	
I _H	I _T =100mA	MAX	MIN	60	40	25	15	mA
dV/dt	V _D =2/3V _{DRM} Gate Open T _j =125°C	MIN	MIN	1000	500	200	100	V/μs

4 Quadrants

Symbol	Test Condition	Quadrant		Value		Unit	
				B	C		
I _{GT}	V _D =12V R _L =33Ω	I - II -III	MAX	50	25	mA	
		IV		70	50		
V _{GT}	ALL	MAX	1.5				
V _{GD}		MIN	0.2				
I _L	I _G =1.2I _{GT}	I -III-IV	MAX	70	50	mA	
		II		100	80		
I _H	I _T =100mA	MAX	MIN	60	40	mA	
dV/dt	V _D =2/3V _{DRM} Gate Open T _j =125°C	MIN	MIN	500	200	V/μs	

STATIC CHARACTERISTICS

Symbol	Parameter	Value(MAX)			Unit
		-600V	-800V	-1200V	
V_{TM}	$I_{TM} = 22.5A$ tp=380μs	$T_j = 25^\circ C$			1.5 V
I_{DRM}	$V_D = V_{DRM}$ $V_R = V_{RRM}$	$T_j = 25^\circ C$	5	5	10 μA
I_{RRM}		$T_j = 125^\circ C$	2	2	1 mA

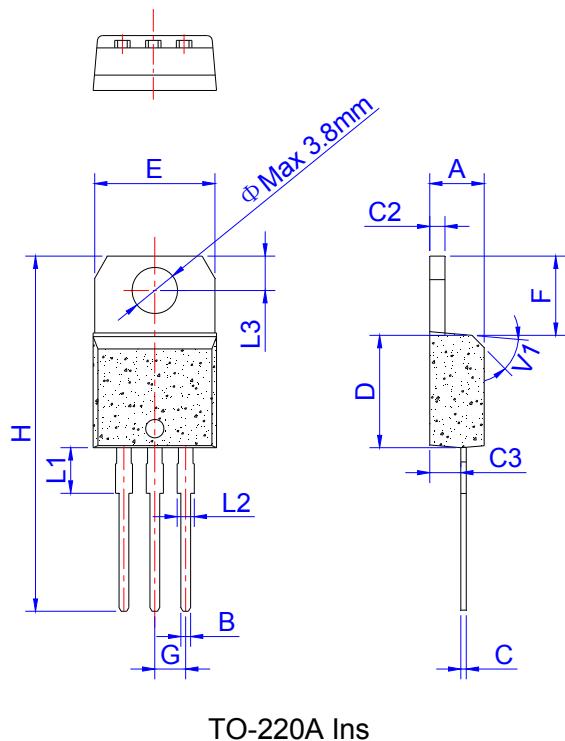
THERMAL RESISTANCES

Symbol	Parameter	Value	Unit
$R_{th(j-c)}$	junction to case(AC)	TO-220A(Ins)	2.1
		TO-220B(Non-Ins)	1.2
		TO-220F(Ins)	2.3
		TO-263	2.5

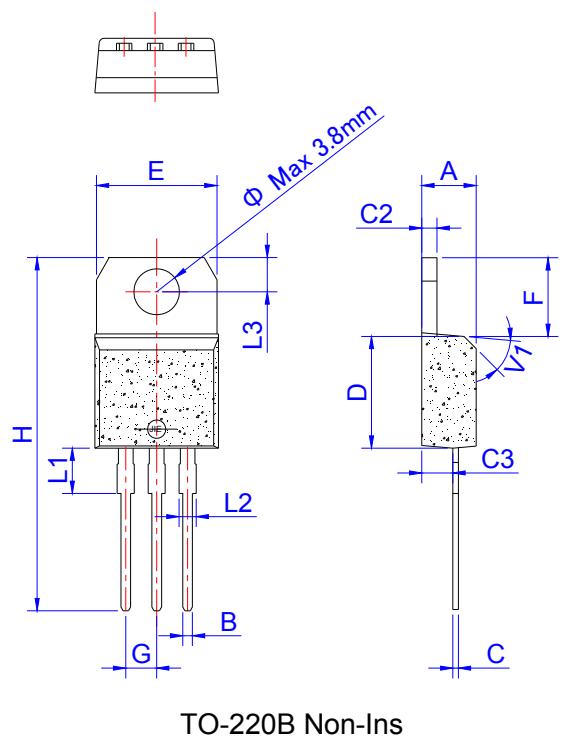
ORDERING INFORMATION

J	ST	16	A	-600	BW
JieJie Microelectronics Co.,Ltd	Triacs	$I_{T(RMS)}: 16A$			BW: $I_{GT1-3} \leq 50mA$ CW: $I_{GT1-3} \leq 35mA$ SW: $I_{GT1-3} \leq 10mA$ TW: $I_{GT1-3} \leq 5mA$ B: $I_{GT1-3} \leq 50mA$ $I_{GT4} \leq 70mA$ C: $I_{GT1-3} \leq 25mA$ $I_{GT4} \leq 50mA$ 600: $V_{DRM} / V_{RRM} \geq 600V$ 800: $V_{DRM} / V_{RRM} \geq 800V$ 1200: $V_{DRM} / V_{RRM} \geq 1200V$

PACKAGE MECHANICAL DATA

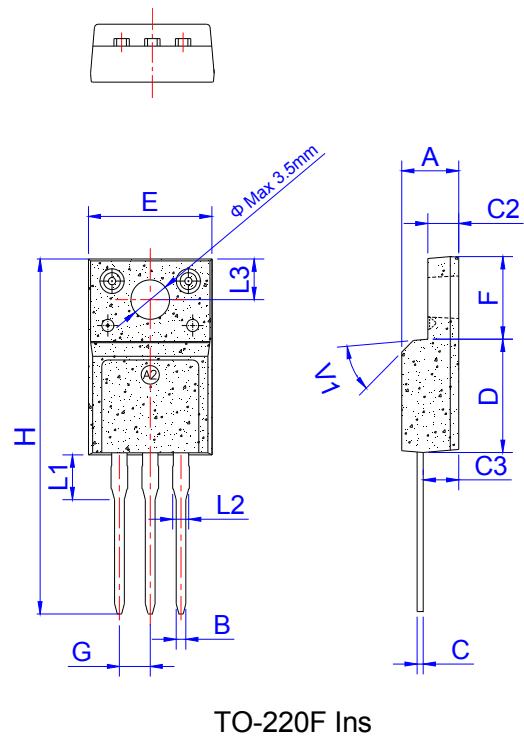


Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	4.40		4.60	0.173		0.181
B	0.61		0.88	0.024		0.035
C	0.46		0.70	0.018		0.028
C2	1.21		1.32	0.048		0.052
C3	2.40		2.72	0.094		0.107
D	8.60		9.70	0.339		0.382
E	9.80		10.4	0.386		0.409
F	6.55		6.95	0.258		0.274
G		2.54			0.1	
H	28.0		29.8	1.102		1.173
L1		3.75			0.148	
L2	1.14		1.70	0.045		0.067
L3	2.65		2.95	0.104		0.116
V1		45°			45°	

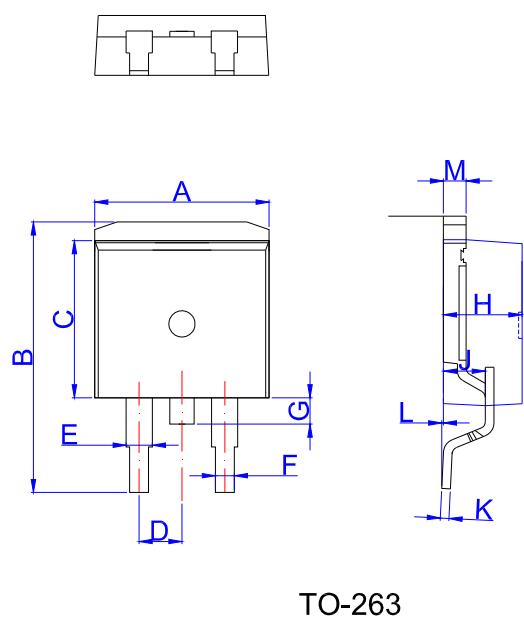


Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	4.40		4.60	0.173		0.181
B	0.61		0.88	0.024		0.035
C	0.46		0.70	0.018		0.028
C2	1.21		1.32	0.048		0.052
C3	2.40		2.72	0.094		0.107
D	8.60		9.70	0.339		0.382
E	9.60		10.4	0.378		0.409
F	6.20		6.60	0.244		0.260
G		2.54			0.1	
H	28.0		29.8	1.102		1.173
L1		3.75			0.148	
L2	1.14		1.70	0.045		0.067
L3	2.65		2.95	0.104		0.116
V1		45°			45°	

PACKAGE MECHANICAL DATA



Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	4.50		4.90	0.177		0.193
B	0.74	0.80	0.83	0.029	0.031	0.033
C	0.47		0.65	0.019		0.026
C2	2.45		2.75	0.096		0.108
C3	2.60		3.00	0.102		0.118
D	8.80		9.30	0.346		0.366
E	9.80		10.4	0.386		0.410
F	6.40		6.80	0.252		0.268
G		2.54			0.1	
H	28.0		29.8	1.102		1.173
L1		3.63			0.143	
L2	1.14		1.70	0.045		0.067
L3		3.30			0.130	
V1		45°			45°	



Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	9.90		10.20	0.390		0.402
B	14.70		15.80	0.579		0.622
C	9.4		9.6	0.37		0.378
D		2.54			0.100	
E	1.20		1.40	0.047		0.055
F	0.75		0.85	0.029		0.033
G			1.75			0.069
H	4.40		4.70	0.173		0.185
J	2.30		2.70	0.091		0.106
K	0.38		0.55	0.015		0.022
L	0	0.10	0.25	0	0.004	0.010
M	1.25		1.35	0.049		0.053

FIG.1 Maximum power dissipation versus RMS on-state current

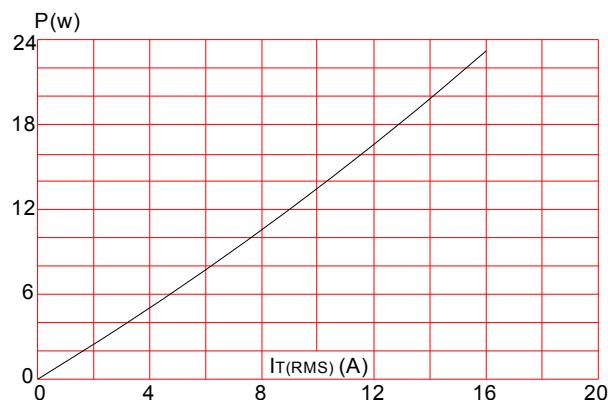


FIG.3: Surge peak on-state current versus number of cycles

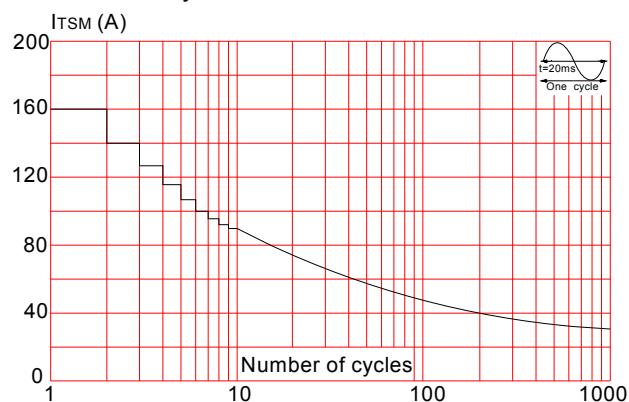


FIG.5: Non-repetitive surge peak on-state current for a sinusoidal pulse with width $t_p < 20\text{ms}$, and corresponding value of I^2t ($dI/dt < 50\text{A}/\mu\text{s}$)

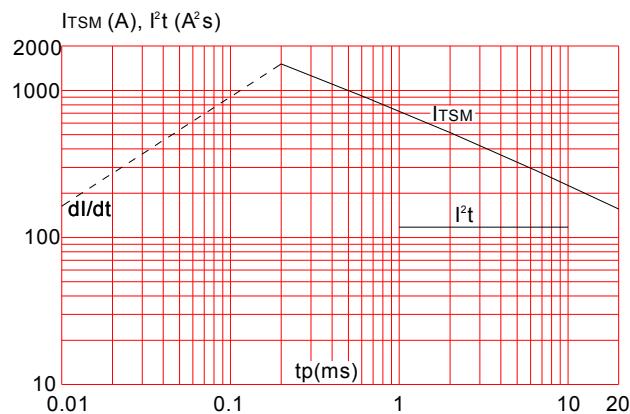


FIG.2: RMS on-state current versus case temperature

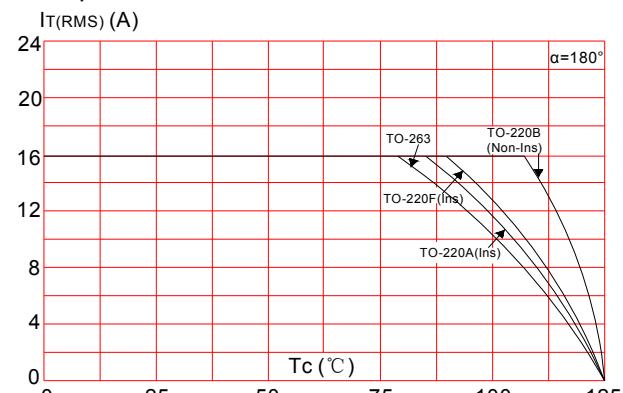


FIG.4: On-state characteristics (maximum values)

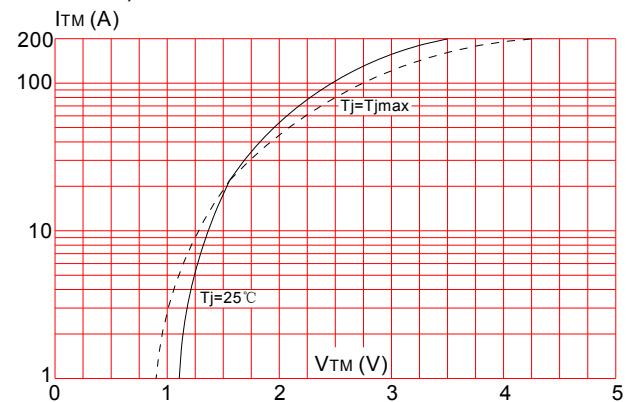
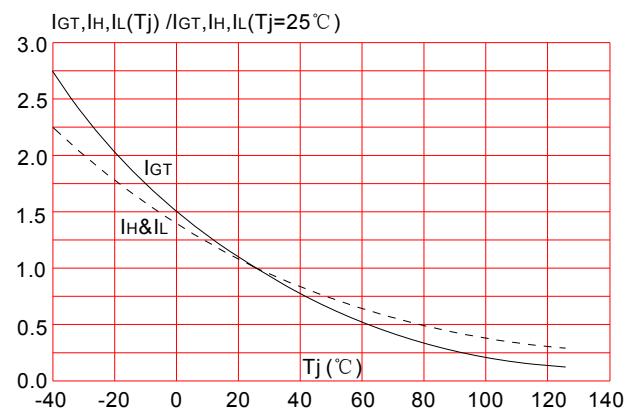


FIG.6: Relative variations of gate trigger current, holding current and latching current versus junction temperature



Information furnished in this document is believed to be accurate and reliable. However, Jiangsu JieJie Microelectronics Co.,Ltd assumes no responsibility for the consequences of use without consideration for such information nor use beyond it.

Information mentioned in this document is subject to change without notice, apart from that when an agreement is signed, Jiangsu JieJie complies with the agreement.

Products and information provided in this document have no infringement of patents. Jiangsu JieJie assumes no responsibility for any infringement of other rights of third parties which may result from the use of such products and information.

This document is the fifth version which is made in 23-Feb.-2018. This document supersedes and replaces all information previously supplied.

 is a registered trademark of Jiangsu JieJie Microelectronics Co.,Ltd.

Copyright ©2018 Jiangsu JieJie Microelectronics Co.,Ltd. Printed All rights reserved.