

# FQD10N20C / FQU10N20C

## N-Channel QFET® MOSFET

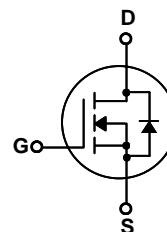
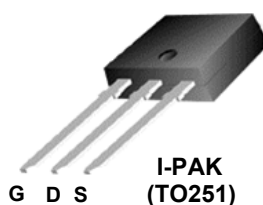
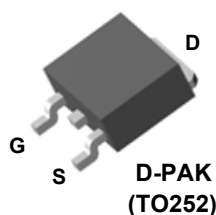
200 V, 7.8 A, 360 mΩ

### Description

This N-Channel enhancement mode power MOSFET is produced using Fairchild Semiconductor®'s proprietary planar stripe and DMOS technology. This advanced MOSFET technology has been especially tailored to reduce on-state resistance, and to provide superior switching performance and high avalanche energy strength. These devices are suitable for switched mode power supplies, active power factor correction (PFC), and electronic lamp ballasts.

### Features

- 7.8 A, 200 V,  $R_{DS(on)} = 360 \text{ m}\Omega$  (Max.)@  $V_{GS} = 10 \text{ V}$ ,  $I_D = 3.9 \text{ A}$
- Low Gate Charge (Typ. 20 nC)
- Low  $C_{rss}$  (Typ. 40.5 pF)
- 100% Avalanche Tested



### Absolute Maximum Ratings $T_C = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	FQD10N20C / FQU10N20C	Unit
$V_{DSS}$	Drain-Source Voltage	200	V
$I_D$	Drain Current - Continuous ( $T_C = 25^\circ\text{C}$ )	7.8	A
	- Continuous ( $T_C = 100^\circ\text{C}$ )	5.0	A
$I_{DM}$	Drain Current - Pulsed (Note 1)	31.2	A
$V_{GSS}$	Gate-Source Voltage	$\pm 30$	V
$E_{AS}$	Single Pulsed Avalanche Energy (Note 2)	210	mJ
$I_{AR}$	Avalanche Current (Note 1)	7.8	A
$E_{AR}$	Repetitive Avalanche Energy (Note 1)	5.0	mJ
$dv/dt$	Peak Diode Recovery $dv/dt$ (Note 3)	5.5	V/ns
$P_D$	Power Dissipation ( $T_C = 25^\circ\text{C}$ )	50	W
	- Derate above $25^\circ\text{C}$	0.4	W/ $^\circ\text{C}$
$T_J, T_{STG}$	Operating and Storage Temperature Range	-55 to +150	$^\circ\text{C}$
$T_L$	Maximum lead temperature for soldering purposes, 1/8" from case for 5 seconds	300	$^\circ\text{C}$

### Thermal Characteristics

Symbol	Parameter	FQD10N20C / FQU10N20C	Unit
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case, Max.	2.5	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient*	50	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient, Max.	110	$^\circ\text{C}/\text{W}$

\* When mounted on the minimum pad size recommended (PCB Mount)

## Electrical Characteristics

$T_C = 25^\circ\text{C}$  unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
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### Off Characteristics

$BV_{DSS}$	Drain-Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$	200	--	--	V
$\Delta BV_{DSS} / \Delta T_J$	Breakdown Voltage Temperature Coefficient	$I_D = 250\text{ }\mu\text{A}$ , Referenced to $25^\circ\text{C}$	--	0.28	--	V/ $^\circ\text{C}$
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = 200\text{ V}, V_{GS} = 0\text{ V}$	--	--	10	$\mu\text{A}$
		$V_{DS} = 160\text{ V}, T_C = 125^\circ\text{C}$	--	--	100	$\mu\text{A}$
$I_{GSSF}$	Gate-Body Leakage Current, Forward	$V_{GS} = 30\text{ V}, V_{DS} = 0\text{ V}$	--	--	100	nA
$I_{GSSR}$	Gate-Body Leakage Current, Reverse	$V_{GS} = -30\text{ V}, V_{DS} = 0\text{ V}$	--	--	-100	nA

### On Characteristics

$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	2.0	--	4.0	V
$R_{DS(on)}$	Static Drain-Source On-Resistance	$V_{GS} = 10\text{ V}, I_D = 3.9\text{ A}$	--	0.29	0.36	$\Omega$
$g_{FS}$	Forward Transconductance	$V_{DS} = 40\text{ V}, I_D = 3.9\text{ A}$	--	5.6	--	S

### Dynamic Characteristics

$C_{iss}$	Input Capacitance	$V_{DS} = 25\text{ V}, V_{GS} = 0\text{ V},$ $f = 1.0\text{ MHz}$	--	395	510	pF
$C_{oss}$	Output Capacitance		--	97	125	pF
$C_{rss}$	Reverse Transfer Capacitance		--	40.5	53	pF

### Switching Characteristics

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 100\text{ V}, I_D = 9.5\text{ A},$ $R_G = 25\text{ }\Omega$	--	11	30	ns
$t_r$	Turn-On Rise Time		--	92	190	ns
$t_{d(off)}$	Turn-Off Delay Time		--	70	150	ns
$t_f$	Turn-Off Fall Time		--	72	160	ns
$Q_g$	Total Gate Charge	$V_{DS} = 160\text{ V}, I_D = 9.5\text{ A},$ $V_{GS} = 10\text{ V}$	--	20	26	nC
$Q_{gs}$	Gate-Source Charge		--	3.1	--	nC
$Q_{gd}$	Gate-Drain Charge		--	10.5	--	nC

### Drain-Source Diode Characteristics and Maximum Ratings

I <sub>S</sub>	Maximum Continuous Drain-Source Diode Forward Current		--	--	7.8	A
I <sub>SM</sub>	Maximum Pulsed Drain-Source Diode Forward Current		--	--	31.2	A
V <sub>SD</sub>	Drain-Source Diode Forward Voltage	V <sub>GS</sub> = 0 V, I <sub>S</sub> = 7.8 A	--	--	1.5	V
t <sub>rr</sub>	Reverse Recovery Time	V <sub>GS</sub> = 0 V, I <sub>S</sub> = 9.5 A, dI <sub>F</sub> / dt = 100 A/μs	--	158	--	ns
Q <sub>rr</sub>	Reverse Recovery Charge		--	0.97	--	μC

#### Notes:

1. Repetitive Rating : Pulse width limited by maximum junction temperature
2.  $L = 5.2\text{ mH}$ ,  $I_{AS} = 7.8\text{ A}$ ,  $V_{DD} = 50\text{ V}$ ,  $R_G = 25\text{ }\Omega$ , Starting  $T_J = 25^\circ\text{C}$
3.  $I_{SD} \leq 9.5\text{ A}$ ,  $di/dt \leq 300\text{ A}/\mu\text{s}$ ,  $V_{DD} \leq BV_{DSS}$ , Starting  $T_J = 25^\circ\text{C}$
4. Essentially independent of operating temperature

## Typical Characteristics

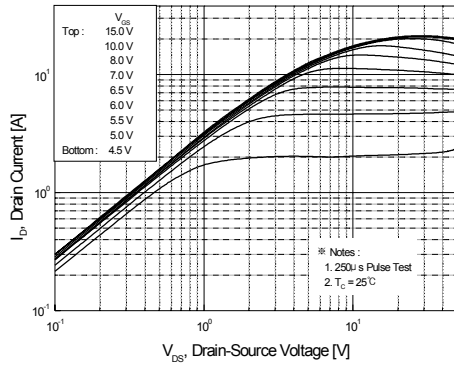


Figure 1. On-Region Characteristics

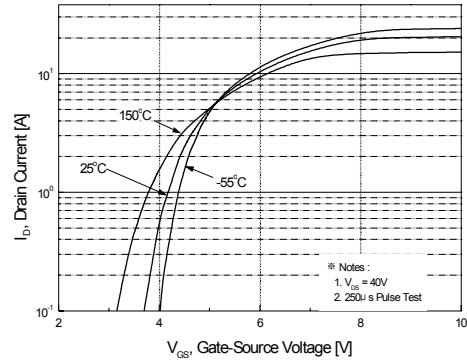


Figure 2. Transfer Characteristics

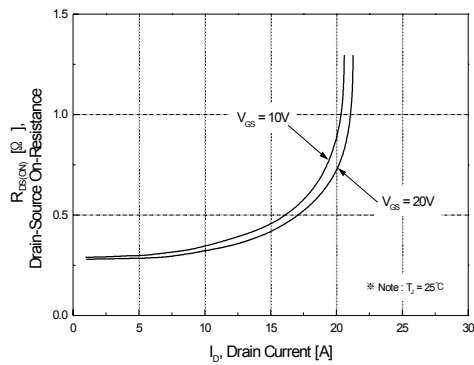


Figure 3. On-Resistance Variation vs Drain Current and Gate Voltage

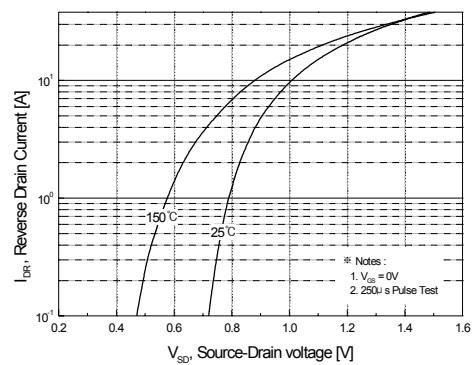


Figure 4. Body Diode Forward Voltage Variation with Source Current and Temperature

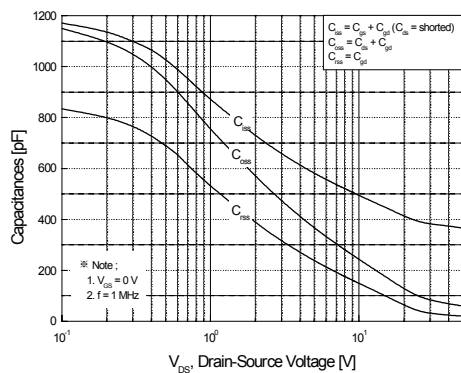


Figure 5. Capacitance Characteristics

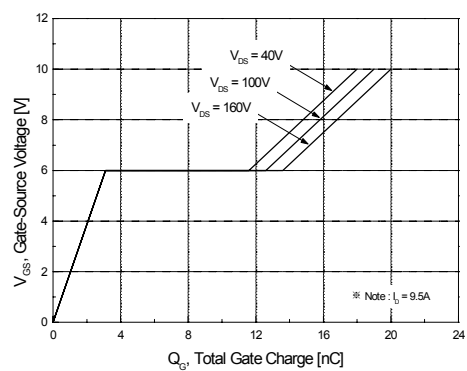


Figure 6. Gate Charge Characteristics

## Typical Characteristics (Continued)

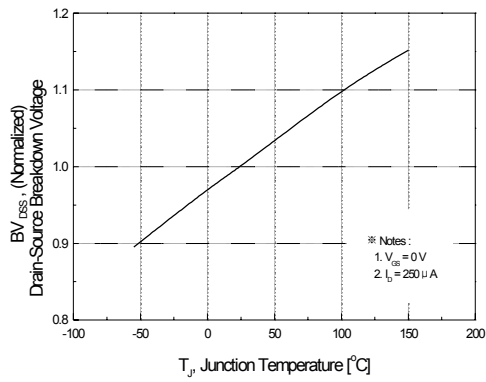


Figure 7. Breakdown Voltage Variation vs Temperature

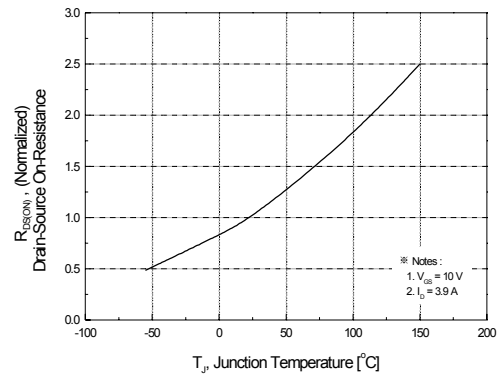


Figure 8. On-Resistance Variation vs Temperature

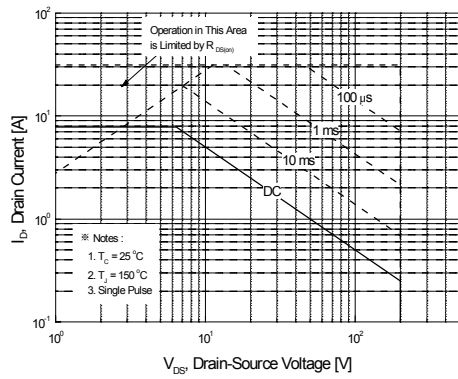


Figure 9. Maximum Safe Operating Area

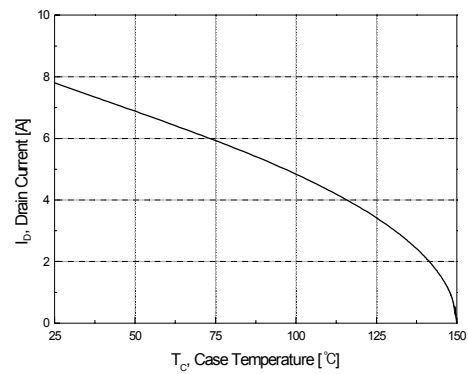


Figure 10. Maximum Drain Current vs Case Temperature

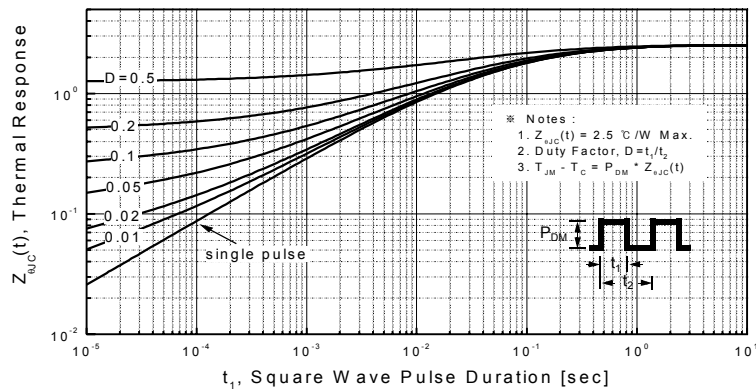
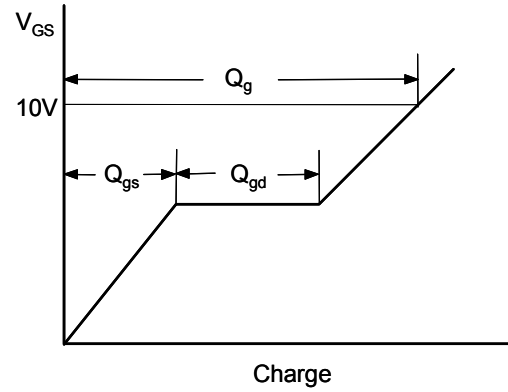
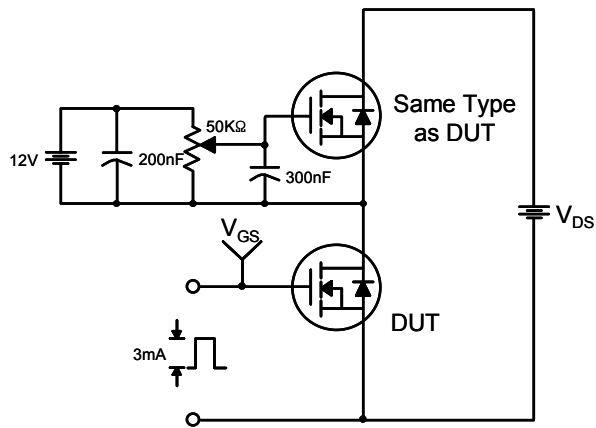
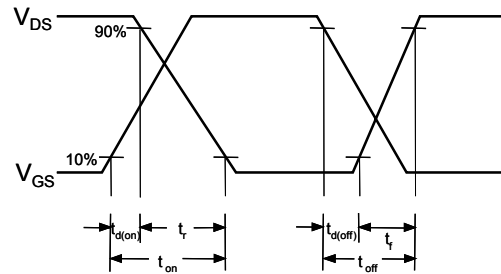
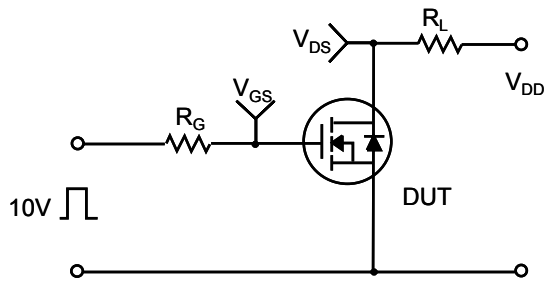


Figure 11. Transient Thermal Response Curve

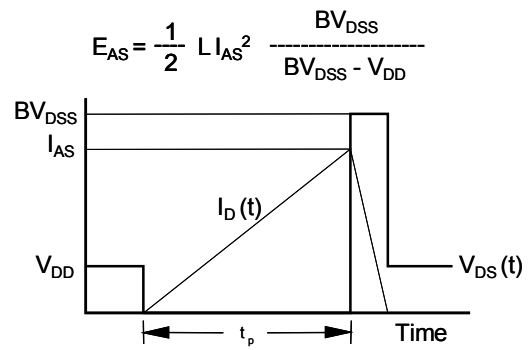
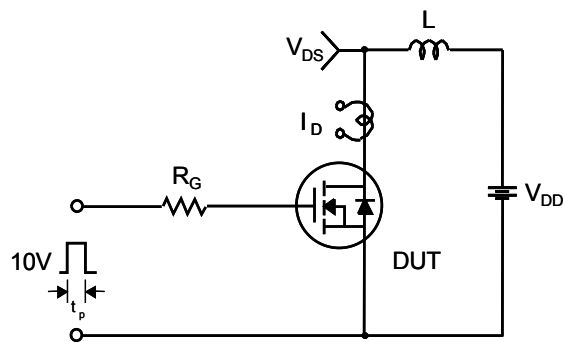
### Gate Charge Test Circuit & Waveform



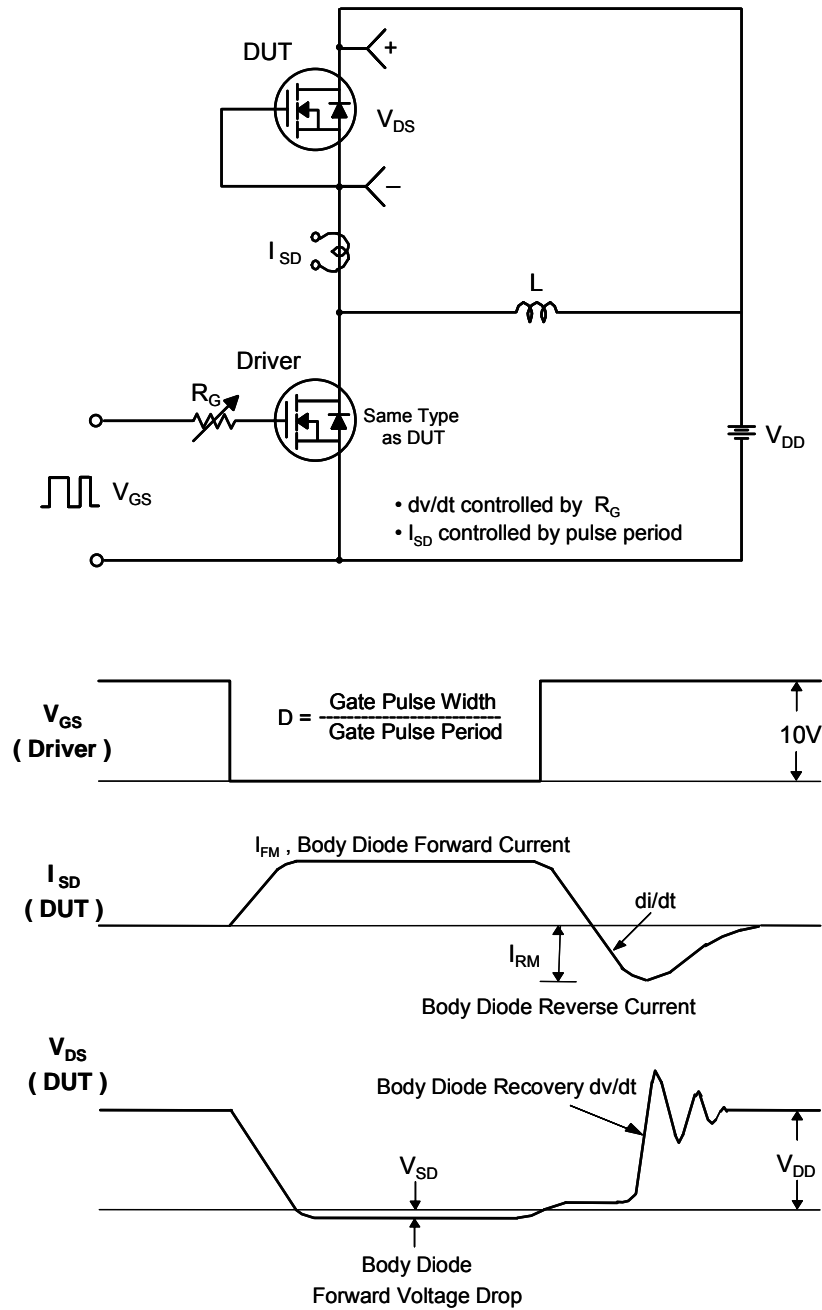
### Resistive Switching Test Circuit & Waveforms



### Unclamped Inductive Switching Test Circuit & Waveforms

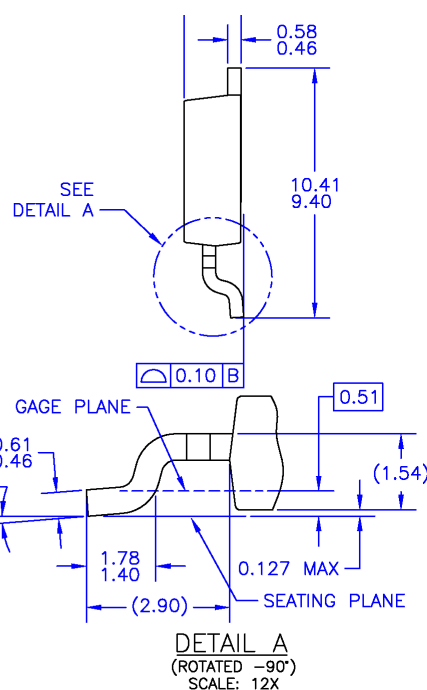
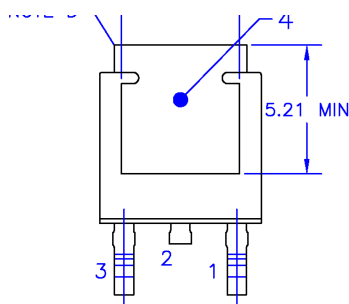
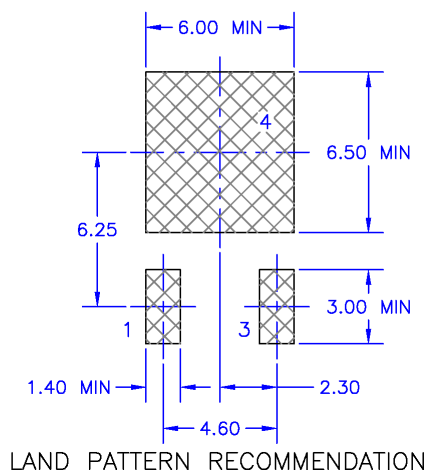
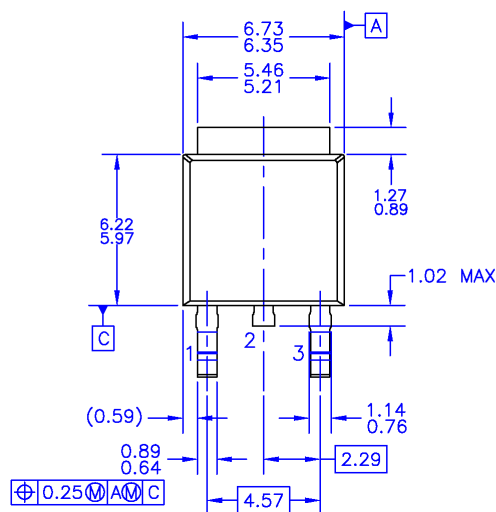


# Peak Diode Recovery dv/dt Test Circuit & Waveforms



# Mechanical Dimensions

## D-PAK



- NOTES: UNLESS OTHERWISE SPECIFIED
- A) THIS PACKAGE CONFORMS TO JEDEC, TO-252, ISSUE C, VARIATION AA.
  - B) ALL DIMENSIONS ARE IN MILLIMETERS.
  - C) DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
  - D) HEAT SINK TOP EDGE COULD BE IN CHAMFERED CORNERS OR EDGE PROTRUSION.
  - E) PRESENCE OF TRIMMED CENTER LEAD IS OPTIONAL.
  - F) DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH AND TIE BAR EXTRUSIONS.
  - G) LAND PATTERN RECOMMENDATION IS BASED ON IPC7351A STD TO220P1003X238-3N.
  - H) DRAWING NUMBER AND REVISION: MKT-T0252A03REV8

### TO-252 (DPAK) MOLDED, 3 LEAD, OPTION AA

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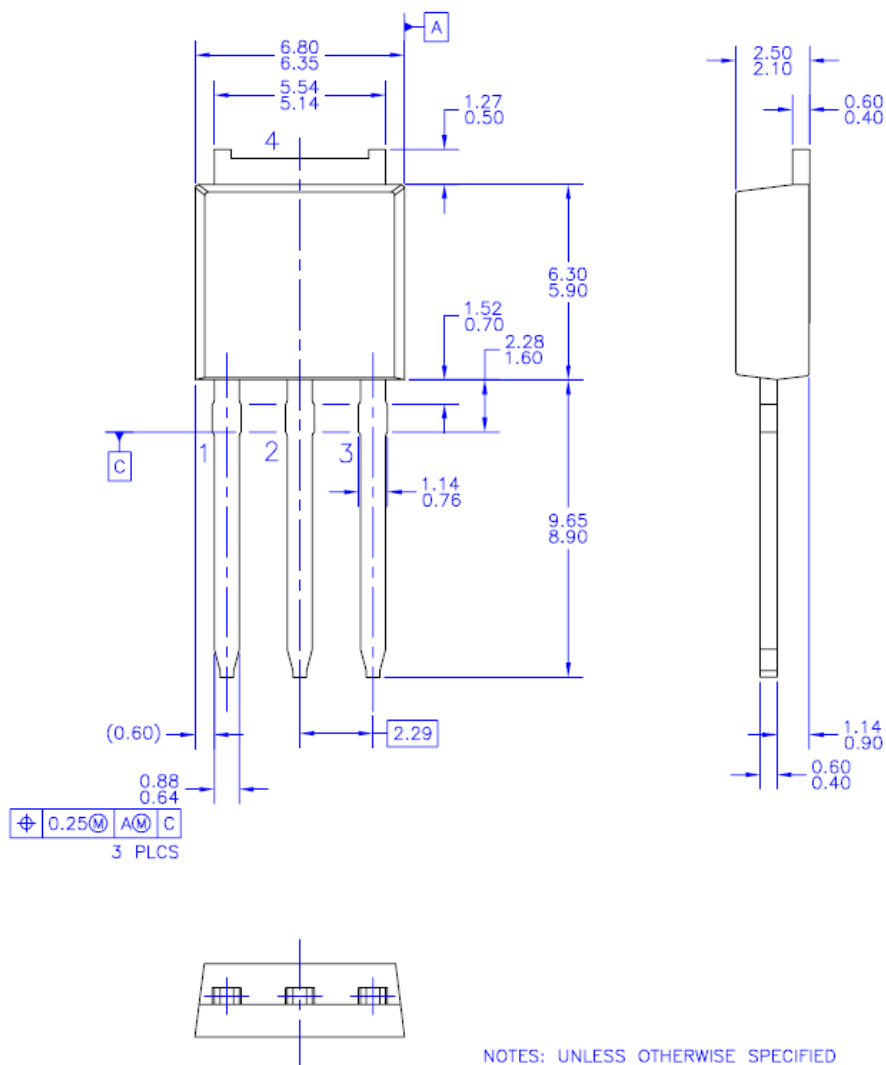
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DIMENSIONS IN MILLIMETERS

# Mechanical Dimensions

## I-PAK



### TO-251 (IPAK) MOLDED, 3LEAD, OPTION AA

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

[http://www.fairchildsemi.com/package/packageDetails.html?id=PN\\_TT251-003](http://www.fairchildsemi.com/package/packageDetails.html?id=PN_TT251-003)

Dimensions in Millimeters



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CTL™	GTO™		TinyPWM™
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Datasheet Identification	Product Status	Definition
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Preliminary	First Production	Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
No Identification Needed	Full Production	Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
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