FAIRCHILD SEMICONDUCTOR®

February 2010

Single-Channel: 6N137M, HCPL2601M, HCPL2611M Dual-Channel: HCPL2630M, HCPL2631M (Preliminary) High Speed 10MBit/s Logic Gate Optocouplers

Features

- Very high speed – 10 MBit/s
- Superior CMR – 10 kV/µs
- Fan-out of 8 over -40°C to +85°C
- Logic gate output
- Strobable output
- Wired OR-open collector
- U.L. recognized (File # E90700, Vol. 2)

Applications

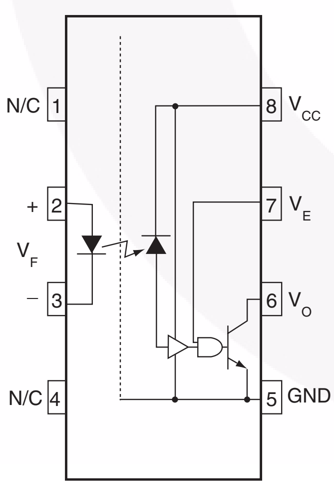
- Ground loop elimination
- LSTTL to TTL, LSTTL or 5-volt CMOS
- Line receiver, data transmission
- Data multiplexing
- Switching power supplies
- Pulse transformer replacement
- Computer-peripheral interface

Description

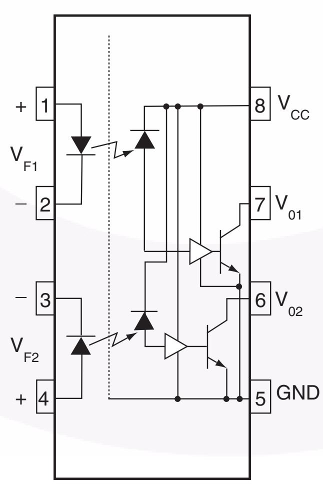
The 6N137M, HCPL2601M, HCPL2611M single-channel and HCPL2630M, HCPL2631M dual-channel optocouplers consist of a 850 nm AlGaAS LED, optically coupled to a very high speed integrated photo-detector logic gate with a strobable output. This output features an open collector, thereby permitting wired OR outputs. The switching parameters are guaranteed over the temperature range of -40°C to +85°C. A maximum input signal of 5mA will provide a minimum output sink current of 13mA (fan out of 8).

An internal noise shield provides superior common mode rejection of typically 10kV/µs. The HCPL2601M and HCPL2631M has a minimum CMR of 5kV/µs. The HCPL2611M has a minimum CMR of 10kV/µs.

Schematics



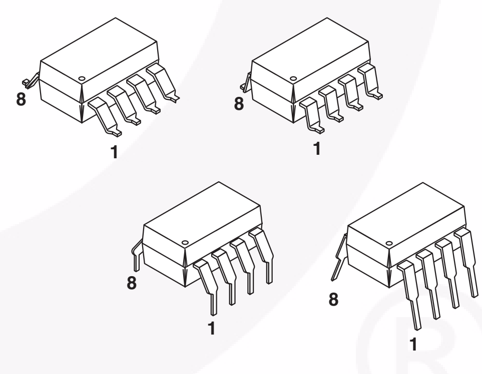
6N137M
HCPL2601M
HCPL2611M



HCPL2630M
HCPL2631M
(Preliminary)

A 0.1µF bypass capacitor must be connected between pins 8 and 5(1).

Package Outlines



Truth Table (Positive Logic)

Input	Enable	Output
H	H	L
L	H	H
H	L	H
L	L	H
H	NC	L
L	NC	H

Absolute Maximum Ratings (T_A = 25°C unless otherwise specified)

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter		Value	Units
T_{STG}	Storage Temperature		-40 to +125	°C
T_{OPR}	Operating Temperature		-40 to +100	°C
T_{SOL}	Lead Solder Temperature		260 for 10 sec	°C
EMITTER				
I_F	DC/Average Forward Input Current	Single Channel	50	mA
		Dual Channel (Each Channel)	30	
V_E	Enable Input Voltage Not to Exceed V_{CC} by more than 500mV	Single Channel	5.5	V
V_R	Reverse Input Voltage	Each Channel	5.0	V
P_I	Power Dissipation	Single Channel	100	mW
		Dual Channel (Each Channel)	45	
DETECTOR				
V_{CC} (1 minute max)	Supply Voltage		7.0	V
I_O	Output Current	Single Channel	50	mA
		Dual Channel (Each Channel)	50	
V_O	Output Voltage	Each Channel	7.0	V
P_O	Collector Output Power Dissipation	Single Channel	85	mW
		Dual Channel (Each Channel)	60	

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to absolute maximum ratings.

Symbol	Parameter	Min.	Max.	Units
I_{FL}	Input Current, Low Level	0	250	µA
I_{FH}	Input Current, High Level	*6.3	15	mA
V_{CC}	Supply Voltage, Output	4.5	5.5	V
V_{EL}	Enable Voltage, Low Level	0	0.8	V
V_{EH}	Enable Voltage, High Level	2.0	V_{CC}	V
T_A	Low Level Supply Current	-40	+85	°C
N	Fan Out (TTL load)		8	

*6.3mA is a guard banded value which allows for at least 20% CTR degradation. Initial input current threshold value is 5.0mA or less.

Electrical Characteristics (T_A = 0 to 70°C unless otherwise specified)

Individual Component Characteristics

Symbol	Parameter	Test Conditions		Min.	Typ.*	Max.	Unit
EMITTER							
V_F	Input Forward Voltage	I_F = 10mA				1.8	V
			T_A = 25°C		1.4	1.75	
B_{VR}	Input Reverse Breakdown Voltage	I_R = 10µA		5.0			V
C_{IN}	Input Capacitance	V_F = 0, f = 1MHz			60		pF
$\Delta V_F / \Delta T_A$	Input Diode Temperature Coefficient	I_F = 10mA			-1.4		mV/°C
DETECTOR							
I_{CCH}	High Level Supply Current	V_{CC} = 5.5V, I_F = 0mA, V_E = 0.5V	Single Channel		6	10	mA
			Dual Channel		10	15	
I_{CCL}	Low Level Supply Current	Single Channel	V_{CC} = 5.5V, I_F = 10mA		8	13	mA
		Dual Channel	V_E = 0.5V		14	21	
I_{EL}	Low Level Enable Current	V_{CC} = 5.5V, V_E = 0.5V			-0.7	-1.6	mA
I_{EH}	High Level Enable Current	V_{CC} = 5.5V, V_E = 2.0V			-0.5	-1.6	mA
V_{EH}	High Level Enable Voltage	V_{CC} = 5.5V, I_F = 10mA		2.0			V
V_{EL}	Low Level Enable Voltage	V_{CC} = 5.5V, I_F = 10mA(3)				0.8	V

Switching Characteristics (T_A = -40°C to +85°C, V_{CC} = 5V, I_F = 7.5mA unless otherwise specified)

Symbol	AC Characteristics	Test Conditions		Min.	Typ.*	Max.	Unit
T_{PLH}	Propagation Delay Time to Output HIGH Level	R_L = 350Ω, C_L = 15pF(4) (Fig. 12)	T_A = 25°C	20	40	75	ns
						100	
T_{PHL}	Propagation Delay Time to Output LOW Level	T_A = 25°C(5)		25	40	75	ns
		R_L = 350Ω, C_L = 15pF (Fig. 12)				100	
$\|T_{PHL}-T_{PLH}\|$	Pulse Width Distortion	(R_L = 350Ω, C_L = 15pF (Fig. 12)			1	35	ns
t_r	Output Rise Time (10–90%)	R_L = 350Ω, C_L = 15pF(6) (Fig. 12)			30		ns
t_f	Output Rise Time (90–10%)	R_L = 350Ω, C_L = 15pF(7) (Fig. 12)			10		ns
t_{ELH}	Enable Propagation Delay Time to Output HIGH Level	I_F = 7.5mA, V_{EH} = 3.5V, R_L = 350Ω, C_L = 15pF(8) (Fig. 13)			15		ns
t_{EHL}	Enable Propagation Delay Time to Output LOW Level	I_F = 7.5mA, V_{EH} = 3.5V, R_L = 350Ω, C_L = 15pF(9) (Fig. 13)			15		ns
$\|CM_H\|$	Common Mode Transient Immunity (at Output HIGH Level)	T_A = 25°C, $\|V_{CM}\|$ = 50V (Peak), I_F = 0mA, V_{OH} (Min.) = 2.0V, R_L = 350Ω(10) (Fig. 14)	6N137M, HCPL2630M		10,000		V/µs
			HCPL2601M, HCPL2631M	5000	10,000		
		$\|V_{CM}\|$ = 400V	HCPL2611M	10,000	15,000		V/µs
$\|CM_L\|$	Common Mode Transient Immunity (at Output LOW Level)	R_L = 350Ω, I_F = 7.5mA, V_{OL} (Max.) = 0.8V, T_A = 25°C(11) (Fig. 14)	6N137M, HCPL2630M		10,000		
			HCPL2601M, HCPL2631M	5000	10,000		
		$\|V_{CM}\|$ = 400V	HCPL2611M	10,000	15,000		

Electrical Characteristics (Continued)

Transfer Characteristics (T_A = -40 to +85°C unless otherwise specified)

Symbol	DC Characteristics	Test Conditions	Min.	Typ.*	Max.	Unit
I_{OH}	HIGH Level Output Current	V_{CC} = 5.5V, V_O = 5.5V, I_F = 250µA, V_E = 2.0V(2)			100	µA
V_{OL}	LOW Level Output Current	V_{CC} = 5.5V, I_F = 5mA, V_E = 2.0V, I_{CL} = 13mA(2)		0.4	0.6	V
I_{FT}	Input Threshold Current	V_{CC} = 5.5V, V_O = 0.6V, V_E = 2.0V, I_{OL} = 13mA		3	5	mA

Isolation Characteristics (T_A = -40°C to +85°C unless otherwise specified.)

Symbol	Characteristics	Test Conditions	Min.	Typ.*	Max.	Unit
I_{I-O}	Input-Output Insulation Leakage Current	Relative humidity = 45%, T_A = 25°C, t = 5s, V_{I-O} = 3000 VDC(12)			1.0*	µA
V_{ISO}	Withstand Insulation Test Voltage	RH < 50%, T_A = 25°C, I_{I-O} ≤ 10µA, t = 1 min.(12)	5000			V_{RMS}
R_{I-O}	Resistance (Input to Output)	V_{I-O} = 500V(12)		10^{11}		Ω
C_{I-O}	Capacitance (Input to Output)	f = 1MHz(12)		1		pF

*All Typicals at V_{CC} = 5V, T_A = 25°C

Notes:

1. The V_{CC} supply to each optoisolator must be bypassed by a 0.1µF capacitor or larger. This can be either a ceramic or solid tantalum capacitor with good high frequency characteristic and should be connected as close as possible to the package V_{CC} and GND pins of each device.
2. Each channel.
3. Enable Input – No pull up resistor required as the device has an internal pull up resistor.
4. t_{PLH} – Propagation delay is measured from the 3.75mA level on the HIGH to LOW transition of the input current pulse to the 1.5 V level on the LOW to HIGH transition of the output voltage pulse.
5. t_{PHL} – Propagation delay is measured from the 3.75mA level on the LOW to HIGH transition of the input current pulse to the 1.5 V level on the HIGH to LOW transition of the output voltage pulse.
6. t_r – Rise time is measured from the 90% to the 10% levels on the LOW to HIGH transition of the output pulse.
7. t_f – Fall time is measured from the 10% to the 90% levels on the HIGH to LOW transition of the output pulse.
8. t_{ELH} – Enable input propagation delay is measured from the 1.5V level on the HIGH to LOW transition of the input voltage pulse to the 1.5V level on the LOW to HIGH transition of the output voltage pulse.
9. t_{EHL} – Enable input propagation delay is measured from the 1.5V level on the LOW to HIGH transition of the input voltage pulse to the 1.5V level on the HIGH to LOW transition of the output voltage pulse.
10. CM_H – The maximum tolerable rate of rise of the common mode voltage to ensure the output will remain in the HIGH state (i.e., V_{OUT} > 2.0V). Measured in volts per microsecond (V/µs).
11. CM_L – The maximum tolerable rate of rise of the common mode voltage to ensure the output will remain in the LOW output state (i.e., V_{OUT} < 0.8V). Measured in volts per microsecond (V/µs).
12. Device considered a two-terminal device: Pins 1, 2, 3 and 4 shorted together, and Pins 5, 6, 7 and 8 shorted together.

Typical Performance Curves

Fig. 1 Low Level Output Voltage vs. Ambient Temperature

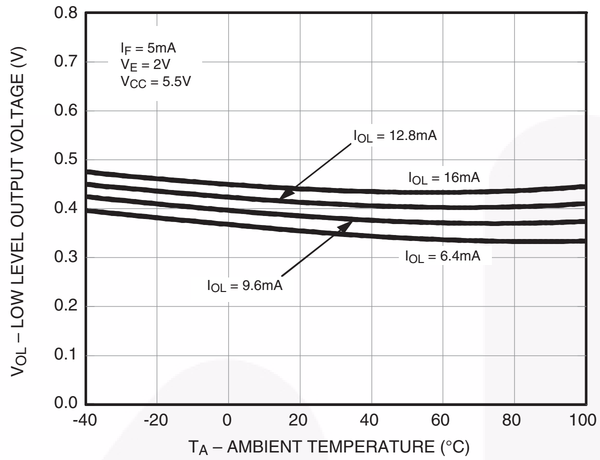


Fig. 2 Input Diode Forward Voltage vs. Forward Current

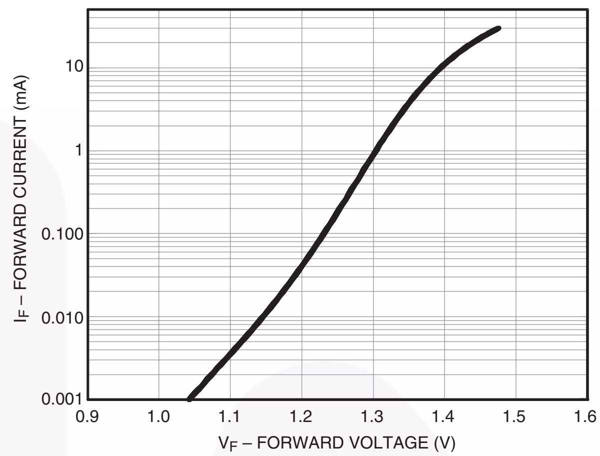


Fig. 3 Switching Time vs. Forward Current

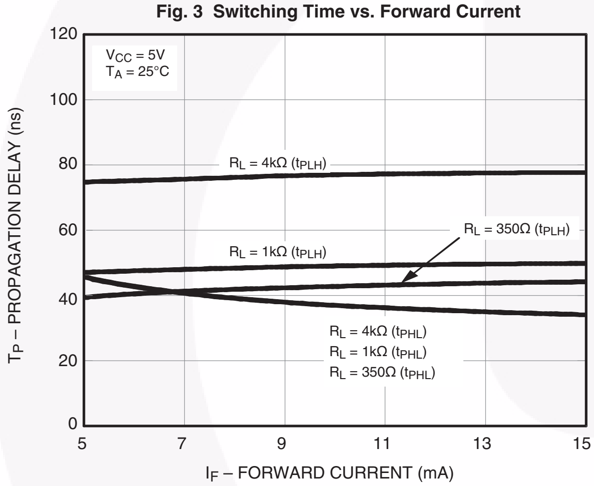


Fig. 4 Low Level Output vs. Ambient Temperature

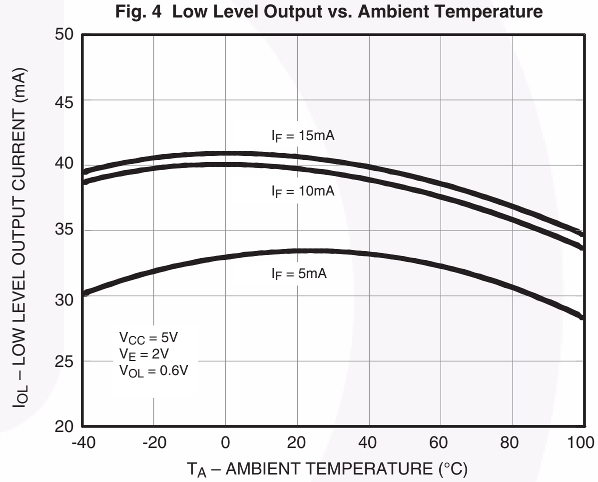


Fig. 5 Input Threshold Current vs. Ambient Temperature

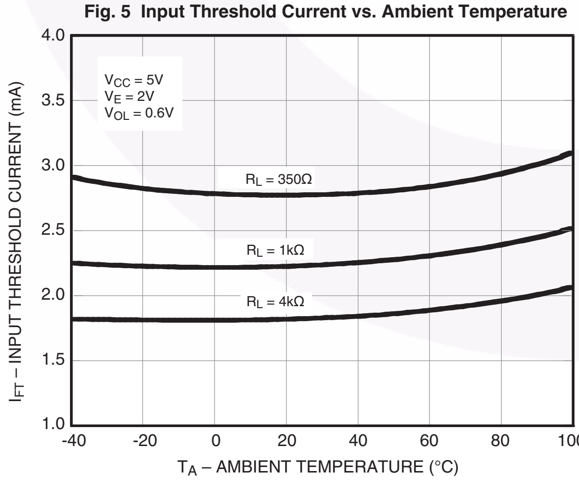
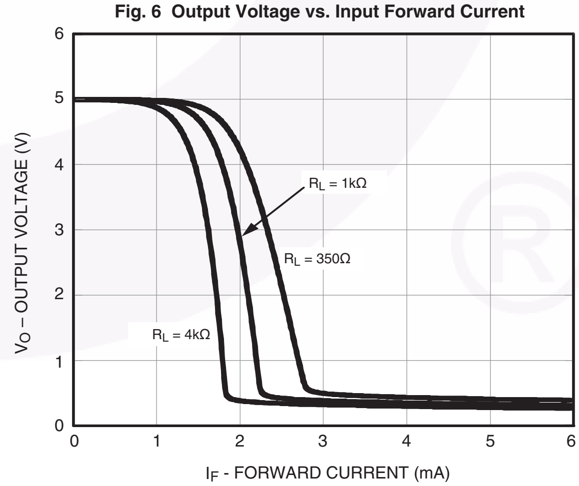


Fig. 6 Output Voltage vs. Input Forward Current



Typical Performance Curves (Continued)

Fig. 7 Pulse Width Distortion vs. Temperature

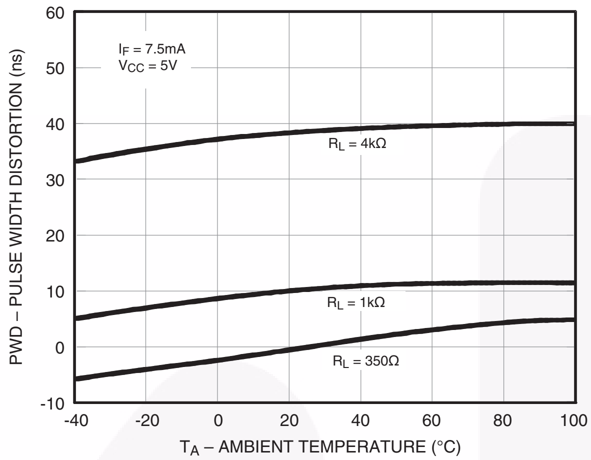


Fig. 8 Rise and Fall Time vs. Temperature

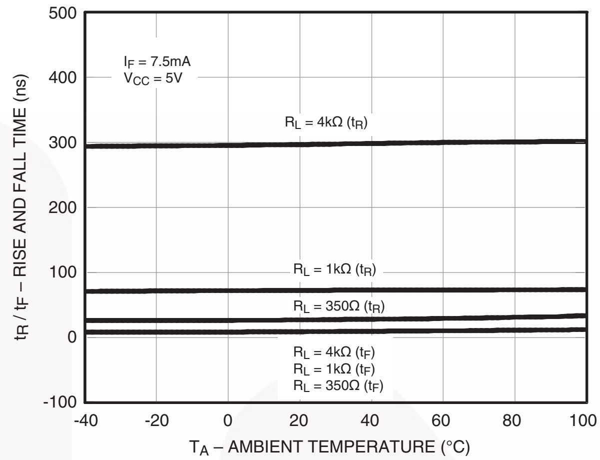


Fig. 9 Enable Propagation Delay vs. Temperature

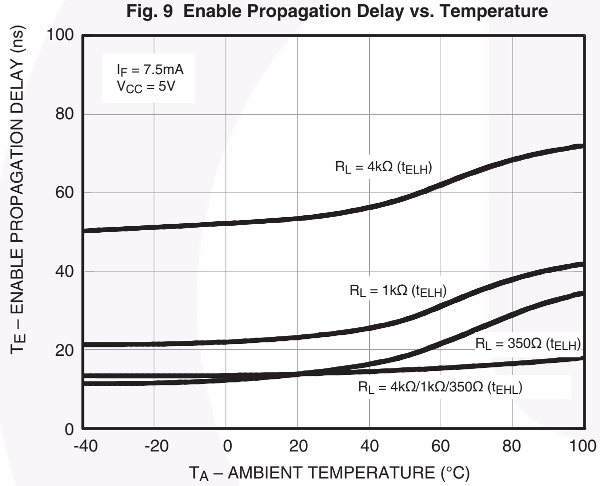


Fig. 10 Switching Time vs. Temperature

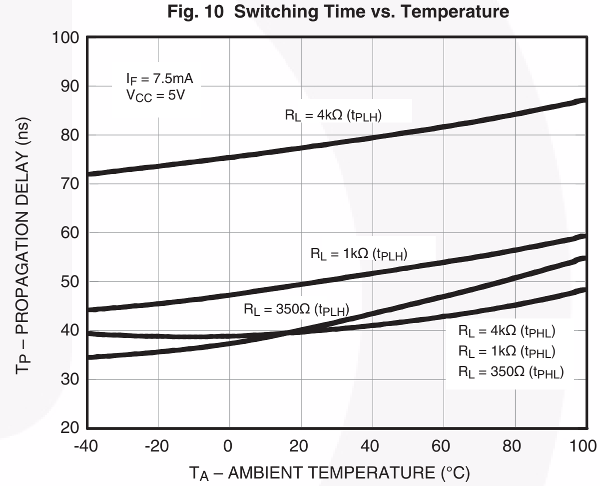
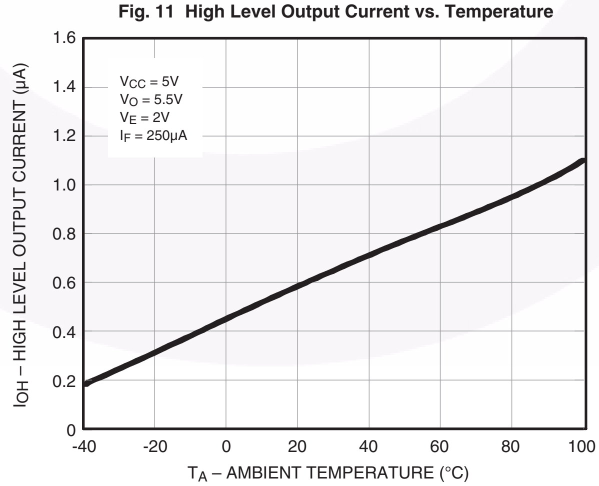


Fig. 11 High Level Output Current vs. Temperature



Test Circuits

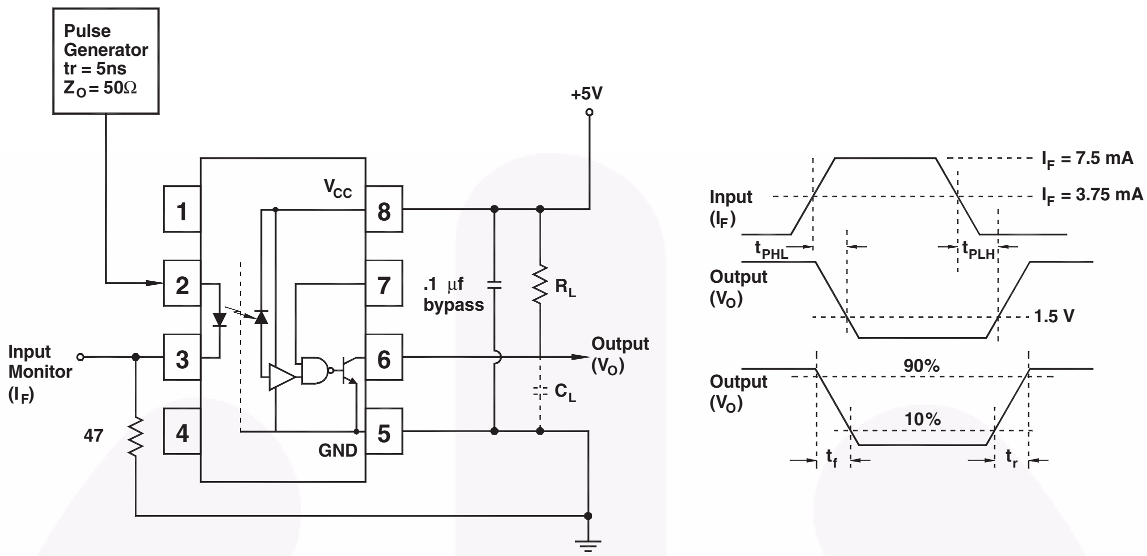


Fig. 12 Test Circuit and Waveforms for t_{PLH}, t_{PHL}, t_r and t_f

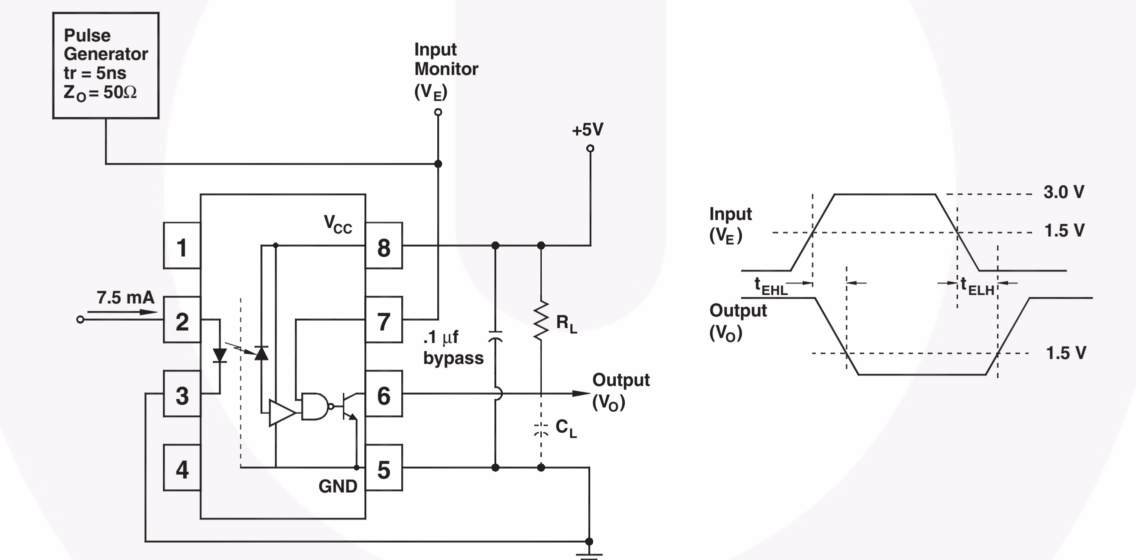


Fig. 13 Test Circuit t_{EHL} and t_{ELH}

Test Circuits (Continued)

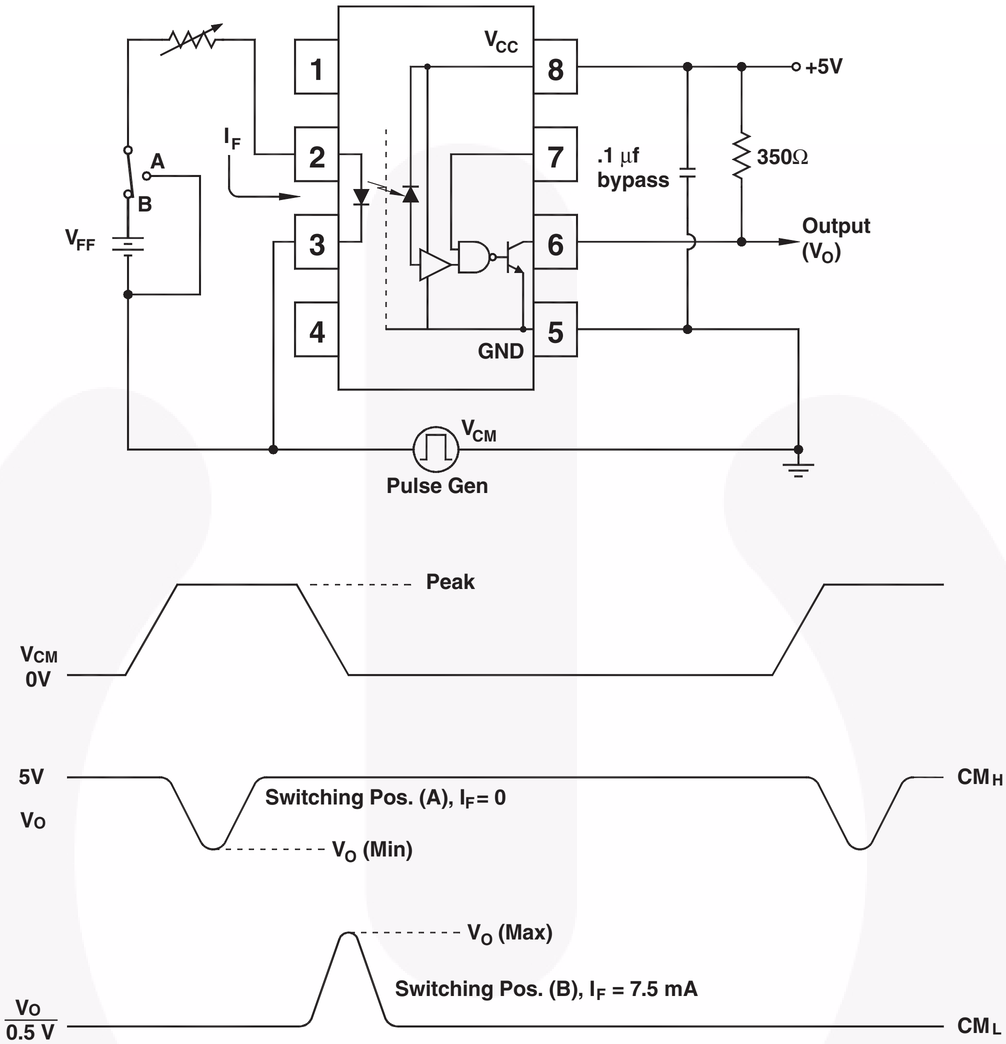
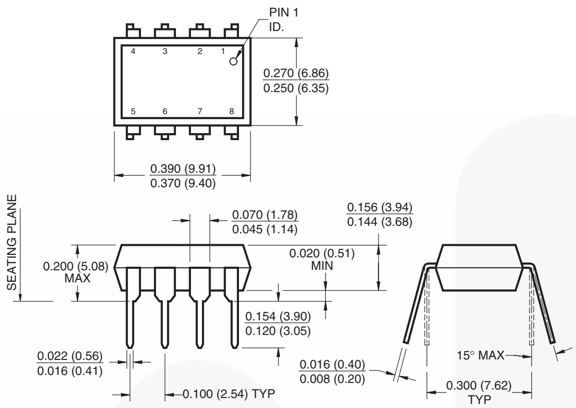


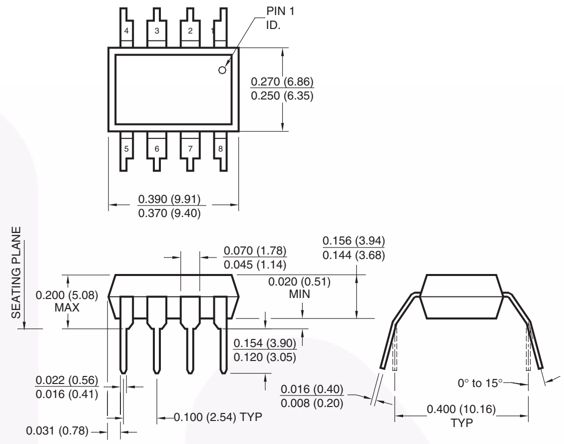
Fig. 14 Test Circuit Common Mode Transient Immunity

Package Dimensions

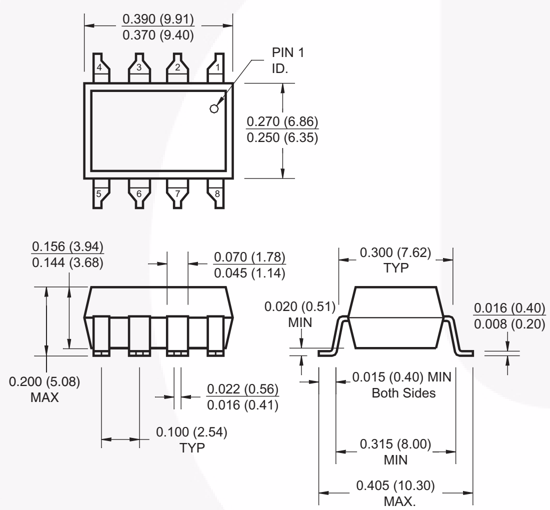
Through Hole



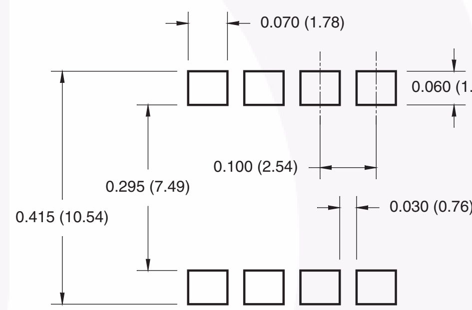
0.4" Lead Spacing (Option TV) (Pending)



Surface Mount – 0.3" Lead Spacing (Option S)



8-Pin Surface Mount DIP – Land Pattern (Option S)



Note:
All dimensions are in inches (millimeters)

Package drawings are provided as a service to customers considering Fairchild components. Drawings may change in any manner without notice. Please note the revision and/or date on the drawing and contact a Fairchild Semiconductor representative to verify or obtain the most recent revision. Package specifications do not expand the terms of Fairchild's worldwide terms and conditions, specifically the warranty therein, which covers Fairchild products.

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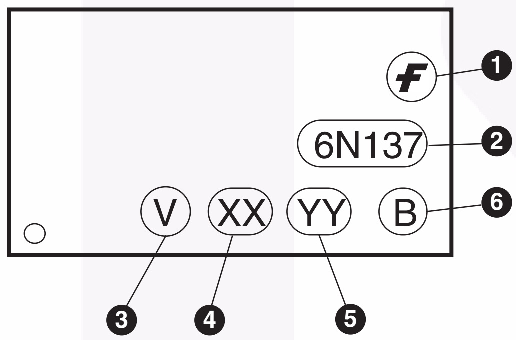
http://www.fairchildsemi.com/packaging/

Ordering Information

Option	Example Part Number	Description
No Suffix	6N137M	Standard Through Hole Device, 50 pcs per tube
S	6N137SM	Surface Mount Lead Bend
SD	6N137SDM	Surface Mount; Tape and Reel
V	6N137VM	IEC60747-5-2 approval pending (VDE)
TV	6N137TVM	IEC60747-5-2 approval pending (VDE), 0.4" lead spacing
SV	6N137SVM	IEC60747-5-2 approval pending (VDE), surface mount
SDV	6N137SDVM	IEC60747-5-2 approval pending (VDE), surface mount, tape and reel

Marking Information

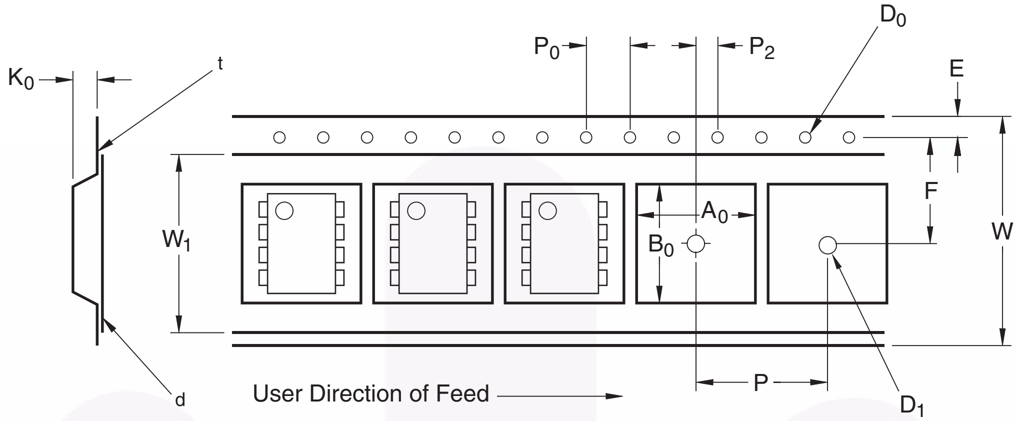


Definitions	
1	Fairchild logo
2	Device number
3	VDE mark (Note: Only appears on parts ordered with VDE option – See order entry table) (pending approval)
4	Two digit year code, e.g., '07'
5	Two digit work week ranging from '01' to '53'
6	Assembly package code

Note:
'HCPL' devices are marked only with the numerical characters (for example, HCPL2630 is marked as '2630').

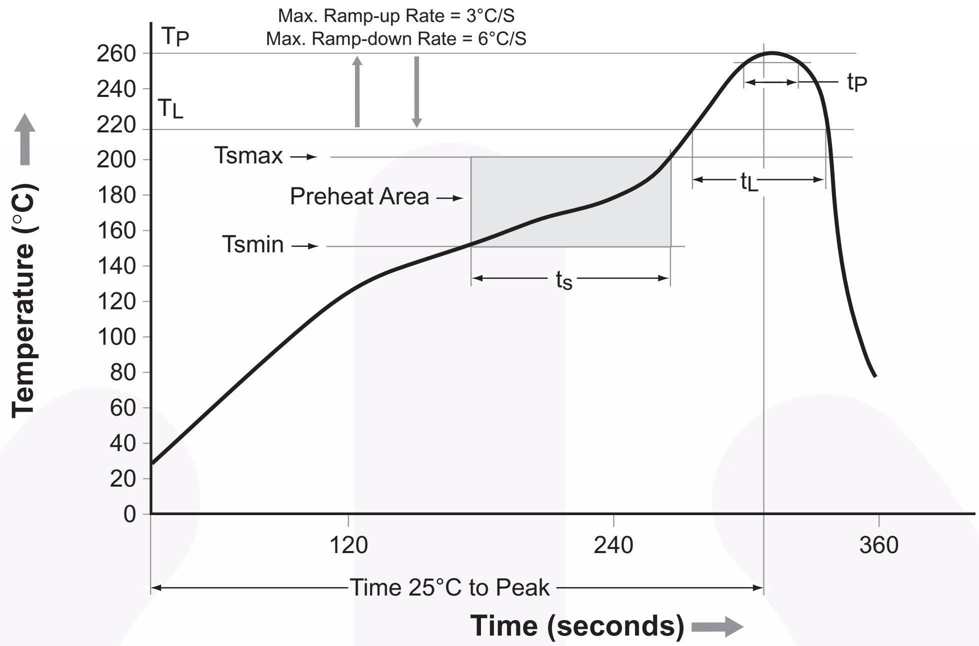
The 'M' suffix on the part number is an order identifier only. It is used to identify orders for the white package version. The 'M' does not appear on the device's top mark.

Carrier Tape Specifications (Option SD)



Symbol	Description	Dimension in mm
W	Tape Width	16.0 ± 0.3
t	Tape Thickness	0.30 ± 0.05
P_0	Sprocket Hole Pitch	4.0 ± 0.1
D_0	Sprocket Hole Diameter	1.55 ± 0.05
E	Sprocket Hole Location	1.75 ± 0.10
F	Pocket Location	7.5 ± 0.1
P_2		2.0 ± 0.1
P	Pocket Pitch	12.0 ± 0.1
A_0	Pocket Dimensions	10.30 ±0.20
B_0		10.30 ±0.20
K_0		4.90 ±0.20
W_1	Cover Tape Width	13.2 ± 0.2
d	Cover Tape Thickness	0.1 max
	Max. Component Rotation or Tilt	10°
R	Min. Bending Radius	30

Reflow Profile



Profile Freature	Pb-Free Assembly Profile
Temperature Min. (Tsmin)	150°C
Temperature Max. (Tsmax)	200°C
Time (t_S) from (Tsmin to Tsmax)	60–120 seconds
Ramp-up Rate (t_L to t_P)	3°C/second max.
Liquidous Temperature (T_L)	217°C
Time (t_L) Maintained Above (T_L)	60–150 seconds
Peak Body Package Temperature	260°C +0°C / –5°C
Time (t_P) within 5°C of 260°C	30 seconds
Ramp-down Rate (T_P to T_L)	6°C/second max.
Time 25°C to Peak Temperature	8 minutes max.

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FETBench™
FlashWriter®*
FPS™
F-PFS™
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Green FPS™ e-Series™
G*max*™
GTO™
IntelliMAX™
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MicroPak™
MicroPak2™
MillerDrive™
MotionMax™
Motion-SPM™
OptoHiT™
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As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury of the user.
2. A critical component in any component of a life support, device, or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

ANTI-COUNTERFEITING POLICY

Fairchild Semiconductor Corporation's Anti-Counterfeiting Policy. Fairchild's Anti-Counterfeiting Policy is also stated on our external website, www.fairchildsemi.com, under Sales Support.

Counterfeiting of semiconductor parts is a growing problem in the industry. All manufacturers of semiconductor products are experiencing counterfeiting of their parts. Customers who inadvertently purchase counterfeit parts experience many problems such as loss of brand reputation, substandard performance, failed applications, and increased cost of production and manufacturing delays. Fairchild is taking strong measures to protect ourselves and our customers from the proliferation of counterfeit parts. Fairchild strongly encourages customers to purchase Fairchild parts either directly from Fairchild or from Authorized Fairchild Distributors who are listed by country on our web page cited above. Products customers buy either from Fairchild directly or from Authorized Fairchild Distributors are genuine parts, have full traceability, meet Fairchild's quality standards for handling and storage and provide access to Fairchild's full range of up-to-date technical and product information. Fairchild and our Authorized Distributors will stand behind all warranties and will appropriately address any warranty issues that may arise. Fairchild will not provide any warranty coverage or other assistance for parts bought from Unauthorized Sources. Fairchild is committed to combat this global problem and encourage our customers to do their part in stopping this practice by buying direct or from authorized distributors.

PRODUCT STATUS DEFINITIONS

Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative / In Design	Datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
No Identification Needed	Full Production	Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
Obsolete	Not In Production	Datasheet contains specifications on a product that is discontinued by Fairchild Semiconductor. The datasheet is for reference information only.

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