MSP430F261x, MSP430F241x Mixed-Signal Microcontrollers

1 Device Overview

1.1 Features

- Low supply voltage range: 1.8 V to 3.6 V
- Ultra-low power consumption
  - Active mode: 365 µA at 1 MHz, 2.2 V
  - Standby mode (VLO): 0.5 µA
  - Off mode (RAM retention): 0.1 µA
- Wake up from standby mode in less than 1 µs
- 16-bit RISC architecture, 62.5-ns instruction cycle time
- Three-channel internal DMA (MSP430F261x only)
- 12-bit analog-to-digital converter (ADC) with internal reference, sample-and-hold, and autoscan feature
- Dual 12-bit digital-to-analog converters (DACs) with synchronization (MSP430F261x only)
- 16-bit Timer_A with three capture/compare registers
- 16-bit Timer_B with seven capture/compare registers with shadow registers
- On-chip comparator
- Four universal serial communication interfaces (USCIs)
  - USCI_A0 and USCI_A1
    - Enhanced UART supporting automatic baud-rate detection
    - IrDA encoder and decoder
    - Synchronous SPI
  - USCI_B0 and USCI_B1
    - I²C
    - Synchronous SPI
- Supply voltage supervisor and monitor with programmable level detection
- Brownout detector
- Bootloader (BSL)
- Serial onboard programming, no external programming voltage needed, programmable code protection by security fuse
- Family members (also see Device Comparison)
  - MSP430F2416
    - 92KB + 256 bytes flash memory
    - 4KB RAM
  - MSP430F2417
    - 92KB + 256 bytes flash memory
    - 8KB RAM
  - MSP430F2418
    - 116KB + 256 bytes flash memory
    - 8KB RAM
  - MSP430F2419
    - 120KB + 256 bytes flash memory
    - 4KB RAM
  - MSP430F2616
    - 92KB + 256 bytes flash memory
    - 4KB RAM
  - MSP430F2617
    - 92KB + 256 bytes flash memory
    - 8KB RAM
  - MSP430F2618
    - 116KB + 256 bytes flash memory
    - 8KB RAM
  - MSP430F2619
    - 120KB + 256 bytes flash memory
    - 4KB RAM
- Available in 80-pin quad flat pack (LQFP), 64-pin LQFP, and 113-pin ball grid array (nFBGA)

1.2 Applications

- Sensor systems
- Industrial control applications
- Hand-held meters
- Medical imaging applications

1.3 Description

The Texas Instruments MSP430™ family of ultra-low-power microcontrollers consists of several devices featuring different sets of peripherals targeted for various applications. The architecture, combined with five low-power modes is optimized to achieve extended battery life in portable measurement applications. The device features a powerful 16-bit RISC CPU, 16-bit registers, and constant generators that contribute to maximum code efficiency. The calibrated digitally controlled oscillator (DCO) allows wake-up from low-power modes to active mode in less than 1 µs.

The MSP430F261x and MSP430F241x series are microcontroller configurations with two built-in 16-bit timers, a fast 12-bit ADC, a comparator, two 12-bit DACs, four USCI modules, DMA, and up to 64 I/O pins. The MSP430F241x devices are identical to the MSP430F261x devices, with the exception that the DAC12 and the DMA modules are not implemented.

The LQFP-64 package is also available as a nonmagnetic package for medical imaging applications.

For complete module descriptions, see the *MSP430F2xx, MSP430G2xx Family User's Guide*.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE(2)
MSP430F2619TPN	LQFP (80)	12 mm × 12 mm
MSP430F2619TPM	LQFP (64)	10 mm × 10 mm
MSP430F2619TZCA	nFBGA (113)	7 mm × 7 mm
MSP430F2619TZQW(3)	MicroStar Junior™ BGA (113)	7 mm × 7 mm

(1) For the most current part, package, and ordering information, see the *Package Option Addendum* in Section 8, or see the TI website at www.ti.com.
(2) The sizes shown here are approximations. For the package dimensions with tolerances, see the *Mechanical Data* in Section 8.
(3) All orderable part numbers in the ZQW (MicroStar Junior BGA) package have been changed to a status of Last Time Buy. Visit the Product life cycle page for details on this status.

1.4 Functional Block Diagrams

Figure 1-1 through Figure 1-4 show the functional block diagrams.

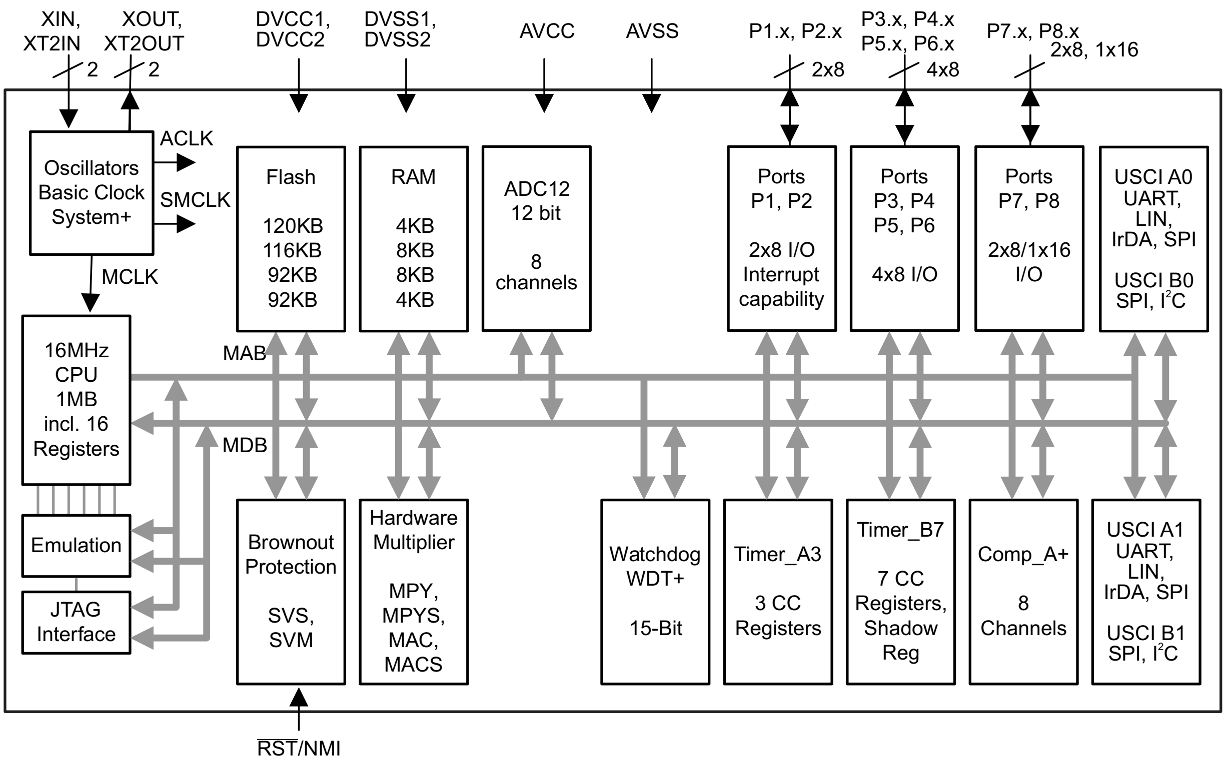

Figure 1-1. MSP430F241x Functional Block Diagram, PN or ZCA or ZQW Package

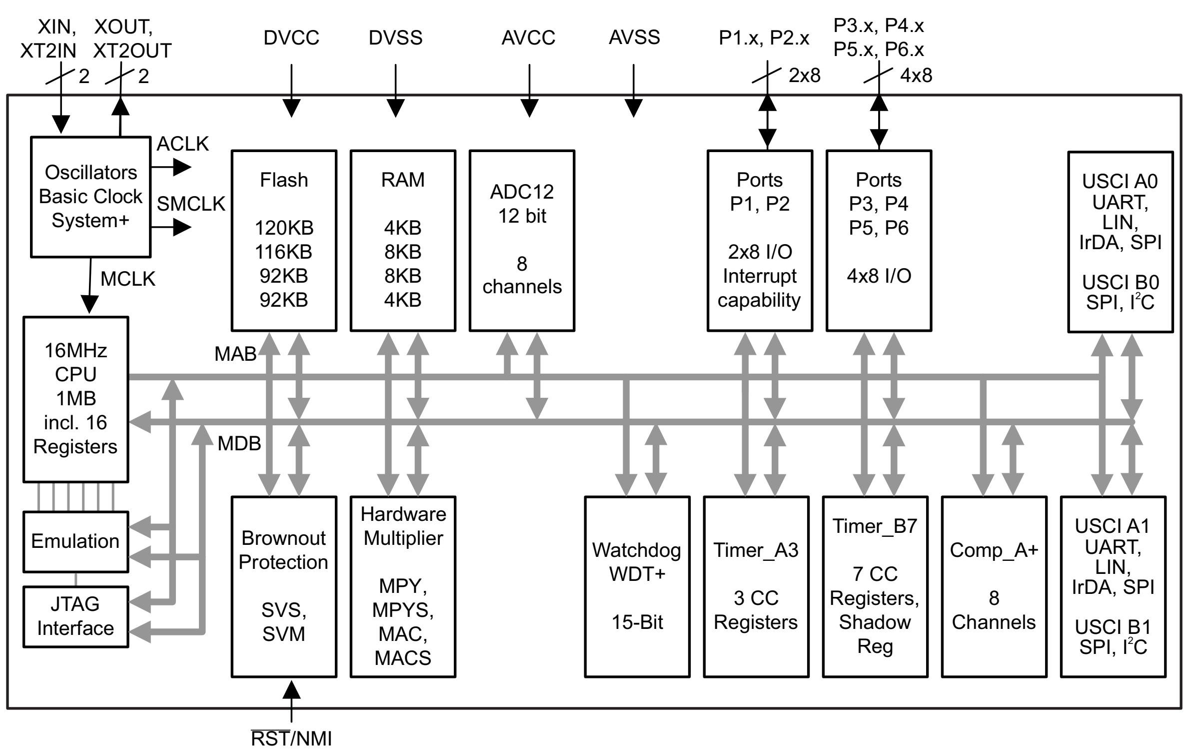

Figure 1-2. MSP430F241x Functional Block Diagram, PM Package

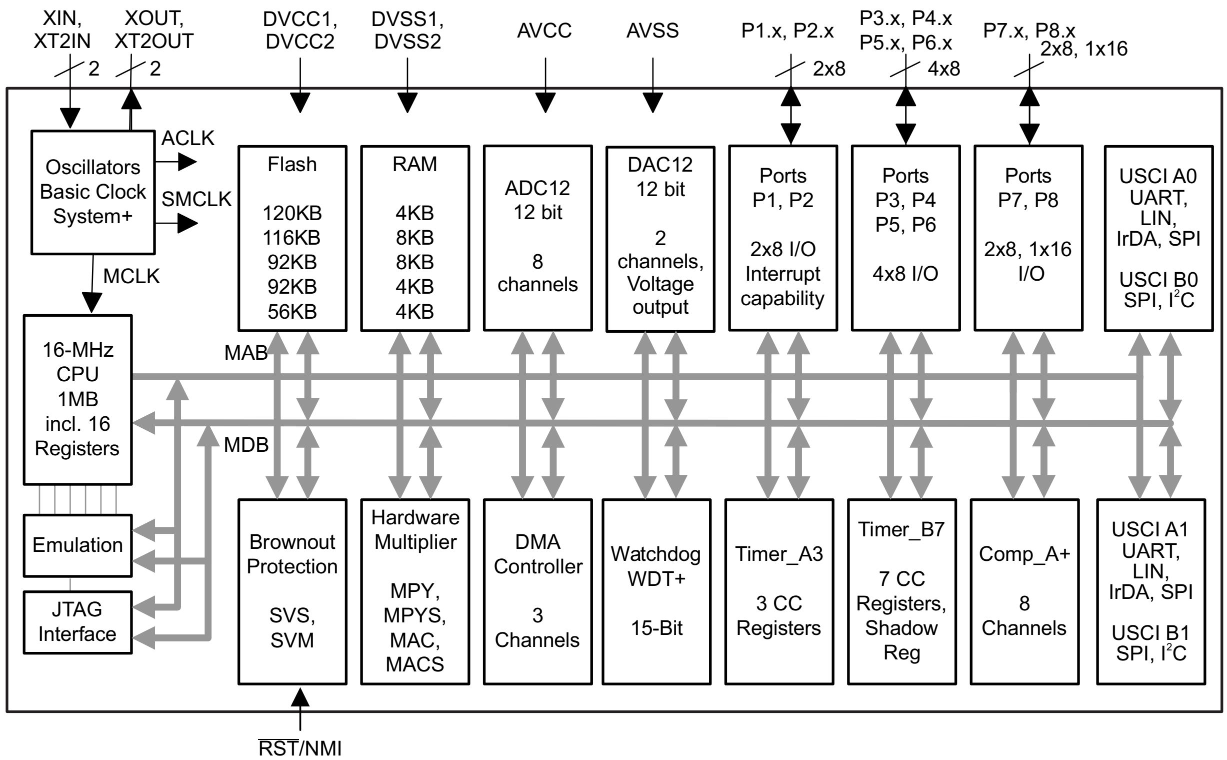

Figure 1-3. MSP430F261x Functional Block Diagram, PN or ZCA or ZQW Package

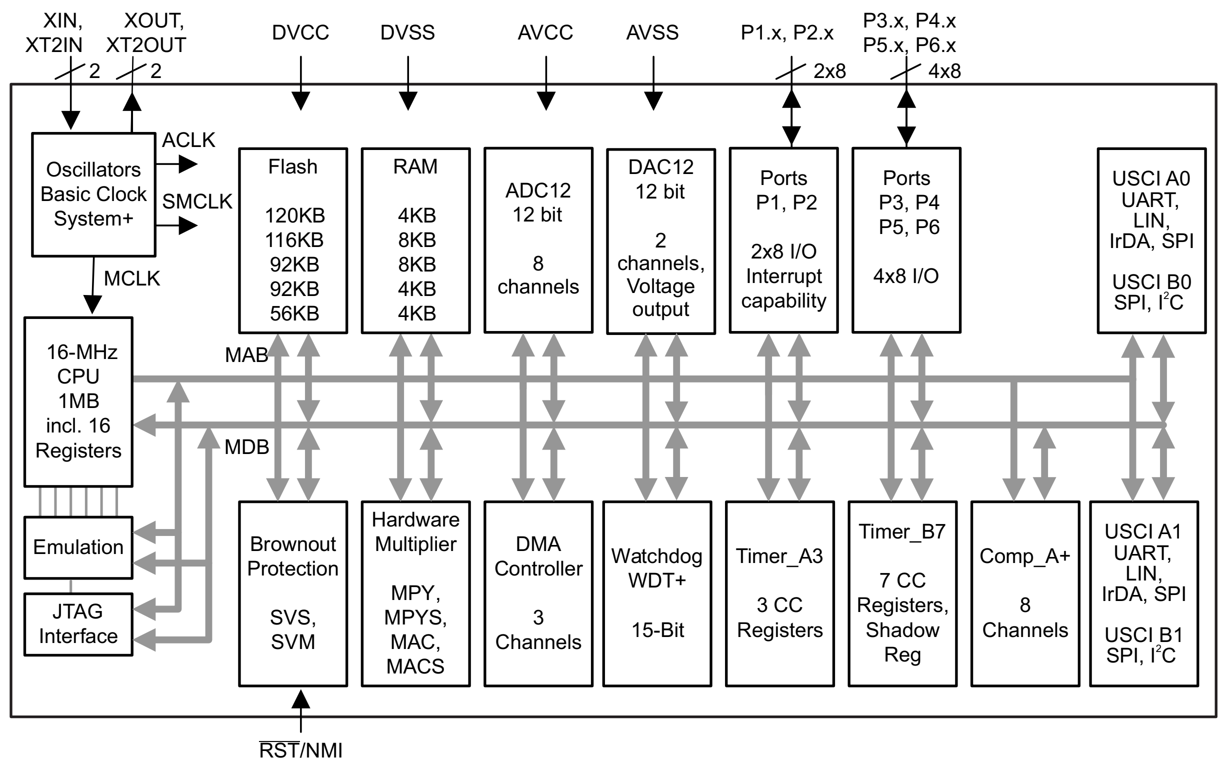

Figure 1-4. MSP430F261x Functional Block Diagram, PM Package

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2 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from revision K to revision L

Changes from November 9, 2012 to May 1, 2020 **Page**

- Format changes throughout document, including addition of section numbering 1
- Throughout the document, added the ZCA package 1
- Added *Device Information* table 2
- Changed the status of all orderable part numbers in the ZQW package 2
- Added Section 1.4 and moved functional block diagrams to it 3
- Added Section 3, *Device Comparison* 9
- Added Section 5 and moved all electrical specifications to it 20
- Added Section 5.2, *ESD Ratings* 20
- Removed "I version" row from T_A row in Section 5.3 (all available devices are "T version" temperature range) 20
- Added separate rows for Information memory segments to Table 6-8, *Memory Organization* 66
- Changed all instances of "bootstrap loader" to "bootloader" 66
- Changed all instances of "INCHx = 0x1010" to "INCHx = 1010b", and corrected all values in the ADDRESS OFFSET column in Table 6-11, *Labels Used by the ADC Calibration Tags* 69
- Corrected P4DIR.x value (changed from 1 to 0) for Timer_B7.TBCLK entry in Table 6-19, *Port P4 (P4.0 to P4.7) Pin Functions* 85
- Added Section 7 and moved *Trademarks* and *Electrostatic Discharge Caution* sections to it 95
- Added Section 8, *Mechanical, Packaging, and Orderable Information* 102

Changes from initial release to revision K

REVISION	COMMENTS
SLAS541K November 2012	Changed P8.6/XT2OUT and P8.7/XT2IN to I/O in Table 4-1
SLAS541J December 2011	Added nonmagnetic package option
SLAS541I July 2011	Changed T_{stg}, Programmed device, to -55°C to 150°C in Section 5.1
SLAS541H May 2011	Changed Control Bits/Signals in Table 6-21, Table 6-22, and Table 6-23 Changed crystal signal names in Table 6-26 and Table 6-27
SLAS541G March 2011	Changed limits on $t_{d(SVSon)}$ parameter
SLAS541F December 2009	Renamed Tags Used by the ADC Calibration Tags table to Tags used by the TLV Structure Changed value of TAG_ADC12_1 from 0x10 to 0x08 in Tags used by the TLV Structure Added CAOUT to P1.0/TACLK, Changed Timer_A3.CCI0A to Timer_A3.CCI1A and Timer_A3.TA0 to Timer_A3.TA1 in P1.2/TA1 row, Changed Timer_A3.CCI0A to Timer_A3.CCI2A and Timer_A3.TA0 to Timer_A3.TA2 in P1.3/TA2 row in Port P1 (P1.0 to P1.7) pin functions table Changed TA0 to Timer_A3.CCI0B in P2.2/CAOUT/TA0/CA4 row of Port P2.0, P2.3, P2.4, P2.6 and P2.7 pin functions table
SLAS541E January 2009	Corrected LFXT1Sx values in Figures 23 and 24 Corrected XT2Sx values in Figures 25 and 26 Corrected $t_{CMErase}$ MIN value from 200 ms to 20 ms and removed two notes in the flash memory table
SLAS541D November 2008	Added the ESD disclaimer Added reserved BGA pins to the terminal function list Corrected the references in the output port parameters Corrected the cumulative program time of the flash

REVISION	COMMENTS
SLAS541C June 2008	Release to market of MSP430F261x BGA devices
SLAS541B May 2008	Added preview of MSP430F261x BGA devices
SLAS541A October 2007	PRODUCTION DATA release Corrected the format and the content shown on the first page Corrected pin number of P3.6 and P3.7 in 64-pin package in the terminal function list Corrected the port schematics Corrected "calibration data" section: typos and formatting corrected Added the figure "typical characteristics - LPM4 current"
SLAS541 June 2007	PRODUCT PREVIEW release

3 Device Comparison

Table 3-1 summarizes the available family members.

Table 3-1. Device Comparison

DEVICE	FLASH (KB)	RAM (KB)	Timer_A	Timer_B	Comp_A+	ADC12	DAC12	DMA	USCI_A	USCI_B	I/O	PACKAGE
MSP430F2619	120	4	1x TA3	1x TB7	Yes	Yes	Yes	Yes	2	2	48 64 64	PM 64 PN 80 ZCA 113 ZQW 113
MSP430F2618	116	8	1x TA3	1x TB7	Yes	Yes	Yes	Yes	2	2	48 64 64	PM 64 PN 80 ZCA 113 ZQW 113
MSP430F2617	92	8	1x TA3	1x TB7	Yes	Yes	Yes	Yes	2	2	48 64 64	PM 64 PN 80 ZCA 113 ZQW 113
MSP430F2616	92	4	1x TA3	1x TB7	Yes	Yes	Yes	Yes	2	2	48 64 64	PM 64 PN 80 ZCA 113 ZQW 113
MSP430F2419	120	4	1x TA3	1x TB7	Yes	Yes	No	No	2	2	48 64 64	PM 64 PN 80 ZCA 113 ZQW 113
MSP430F2418	116	8	1x TA3	1x TB7	Yes	Yes	No	No	2	2	48 64 64	PM 64 PN 80 ZCA 113 ZQW 113
MSP430F2417	92	8	1x TA3	1x TB7	Yes	Yes	No	No	2	2	48 64 64	PM 64 PN 80 ZCA 113 ZQW 113
MSP430F2416	92	4	1x TA3	1x TB7	Yes	Yes	No	No	2	2	48 64 64	PM 64 PN 80 ZCA 113 ZQW 113

3.1 Related Products

For information about other devices in this family of products or related products, see the following links.

16-bit and 32-bit microcontrollers
: High-performance, low-power solutions to enable the autonomous future

Products for MSP430 ultra-low-power sensing & measurement MCUs
: One platform. One ecosystem. Endless possibilities.

Companion products for MSP430F2619
: Review products that are frequently purchased or used with this product.

Reference designs
: Find reference designs leveraging the best in TI technology to solve your system-level challenges

4 Terminal Configuration and Functions

4.1 Pin Diagrams

Figure 4-1 shows the pinout of the 80-pin PN package for the MSP430F241x devices.

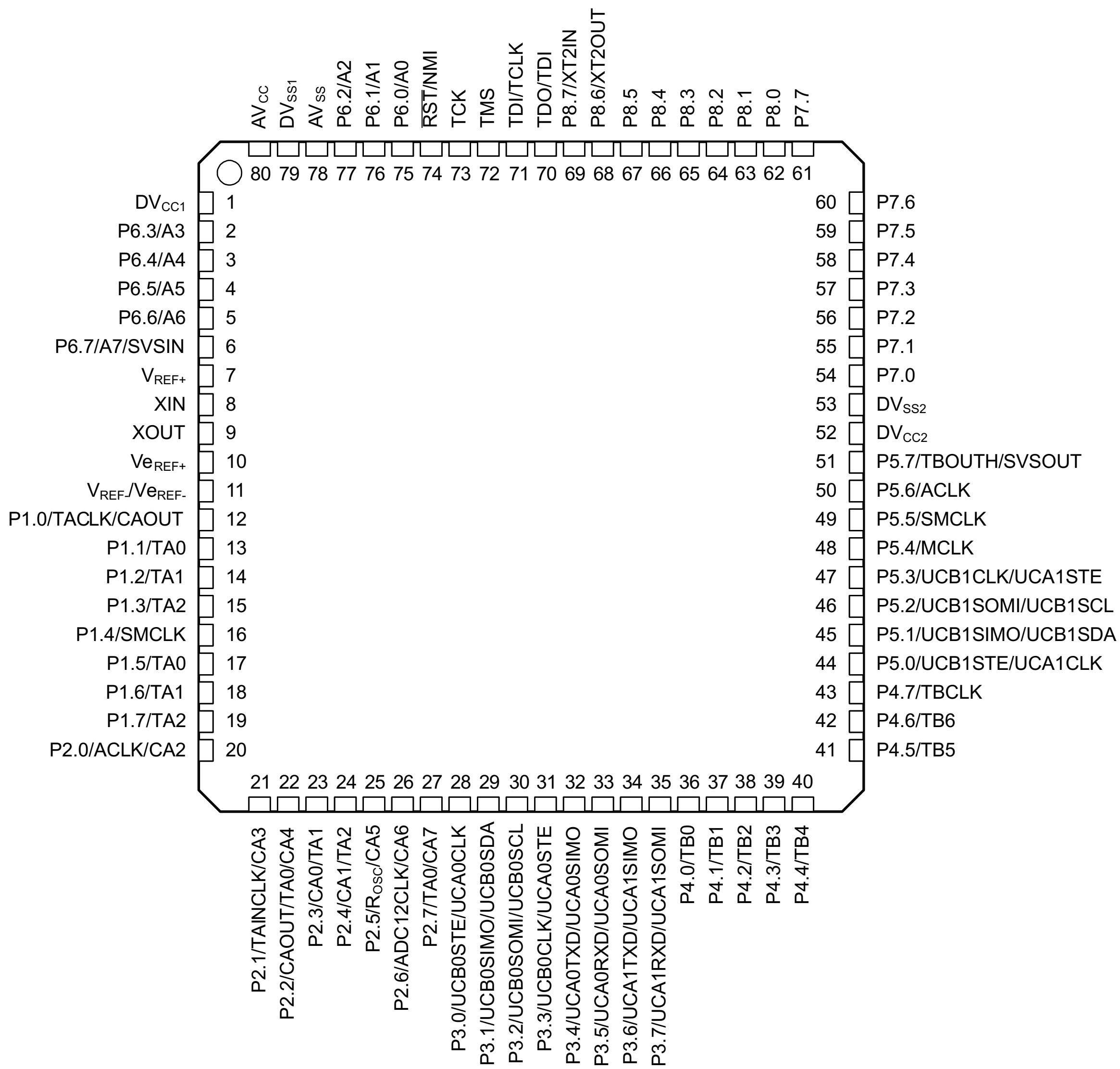


Figure 4-1. 80-Pin PN Package, MSP430F241x (Top View)

Figure 4-2 shows the pinout of the 64-pin PM package for the MSP430F241x devices.

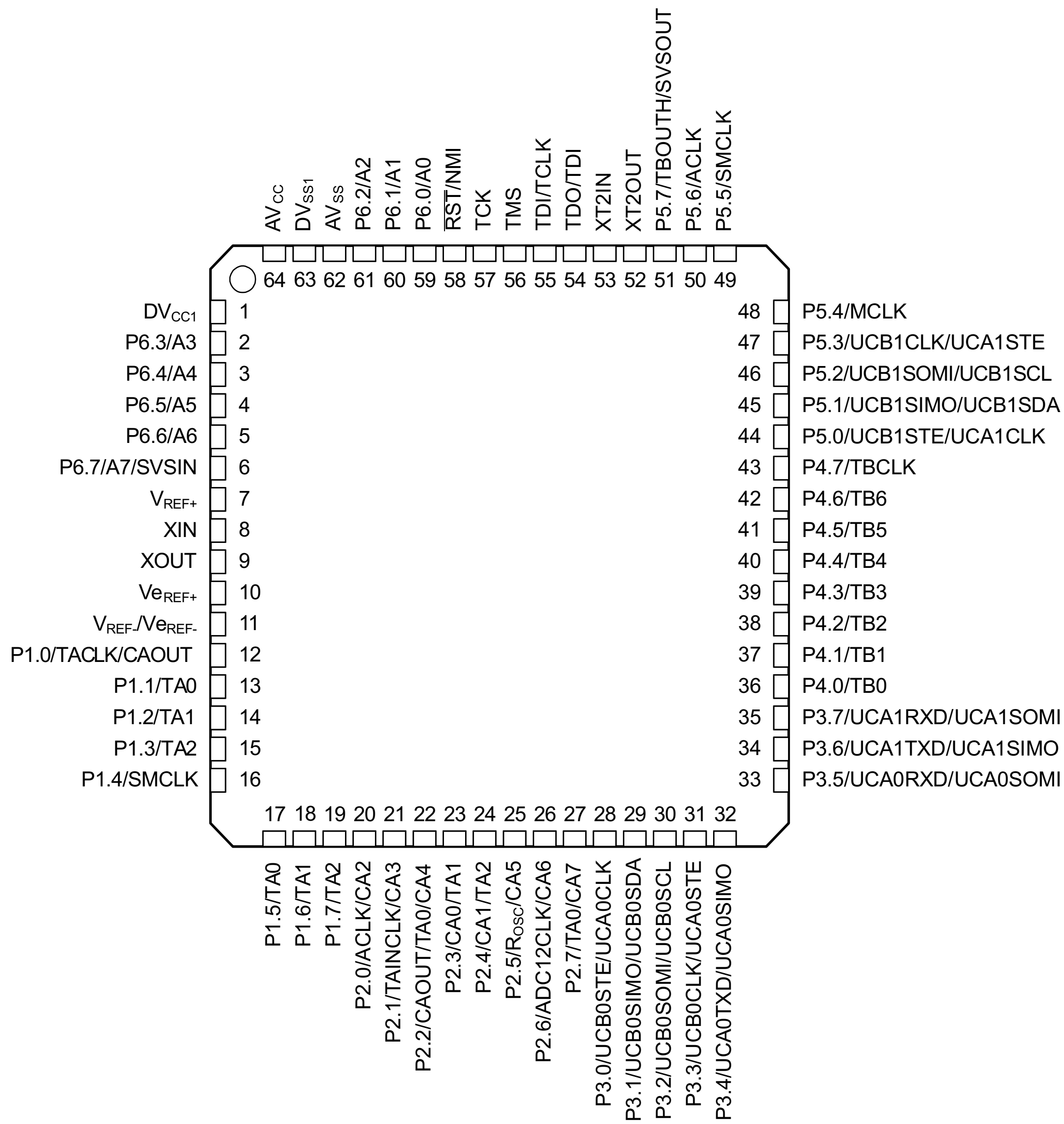


Figure 4-2. 64-Pin PM Package, MSP430F241x (Top View)

Figure 4-3 shows the pinout of the 80-pin PN package for the MSP430F261x devices.

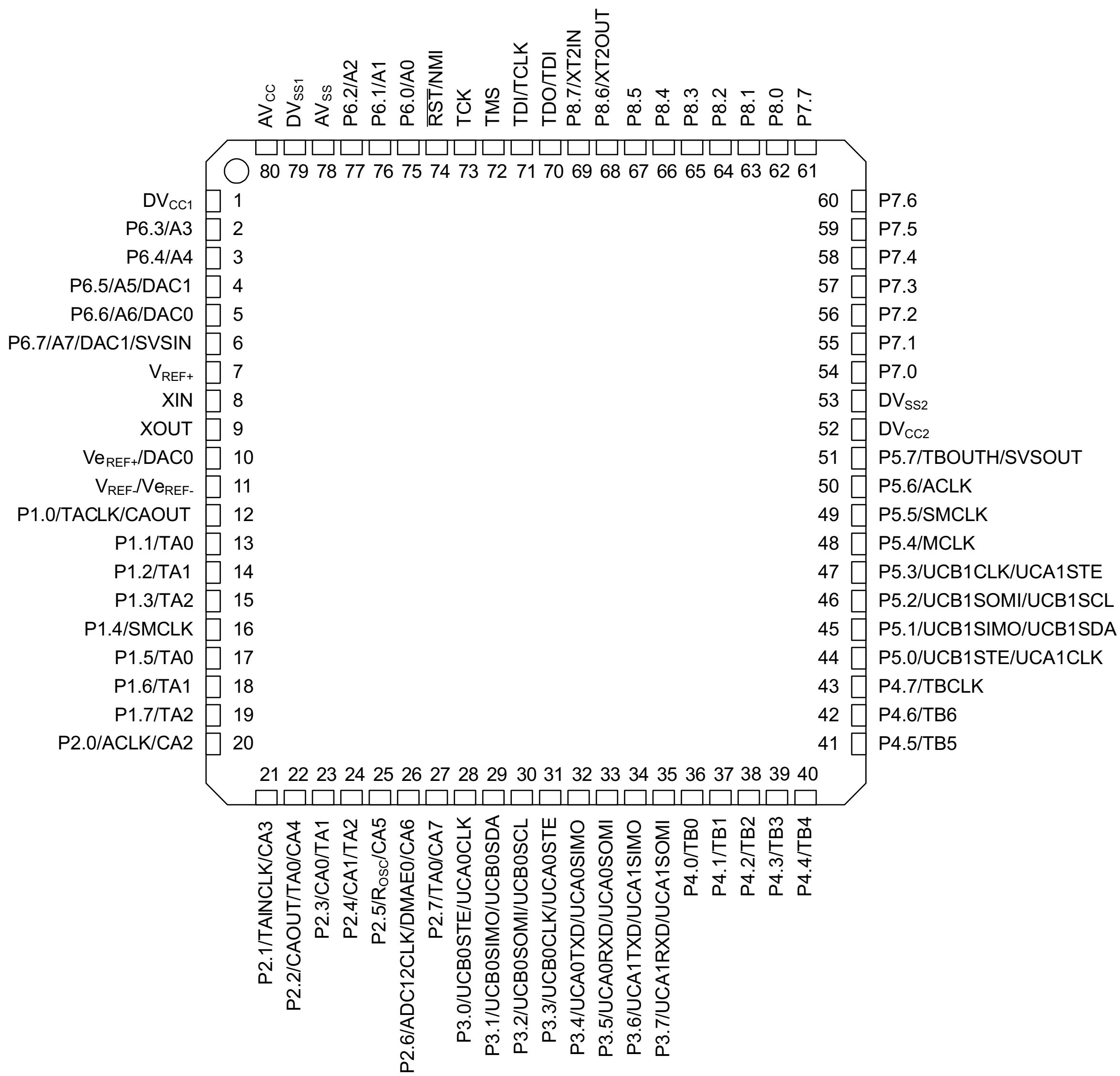


Figure 4-3. 80-Pin PN Package, MSP430F261x (Top View)

Figure 4-4 shows the pinout of the 64-pin PM package for the MSP430F261x devices.

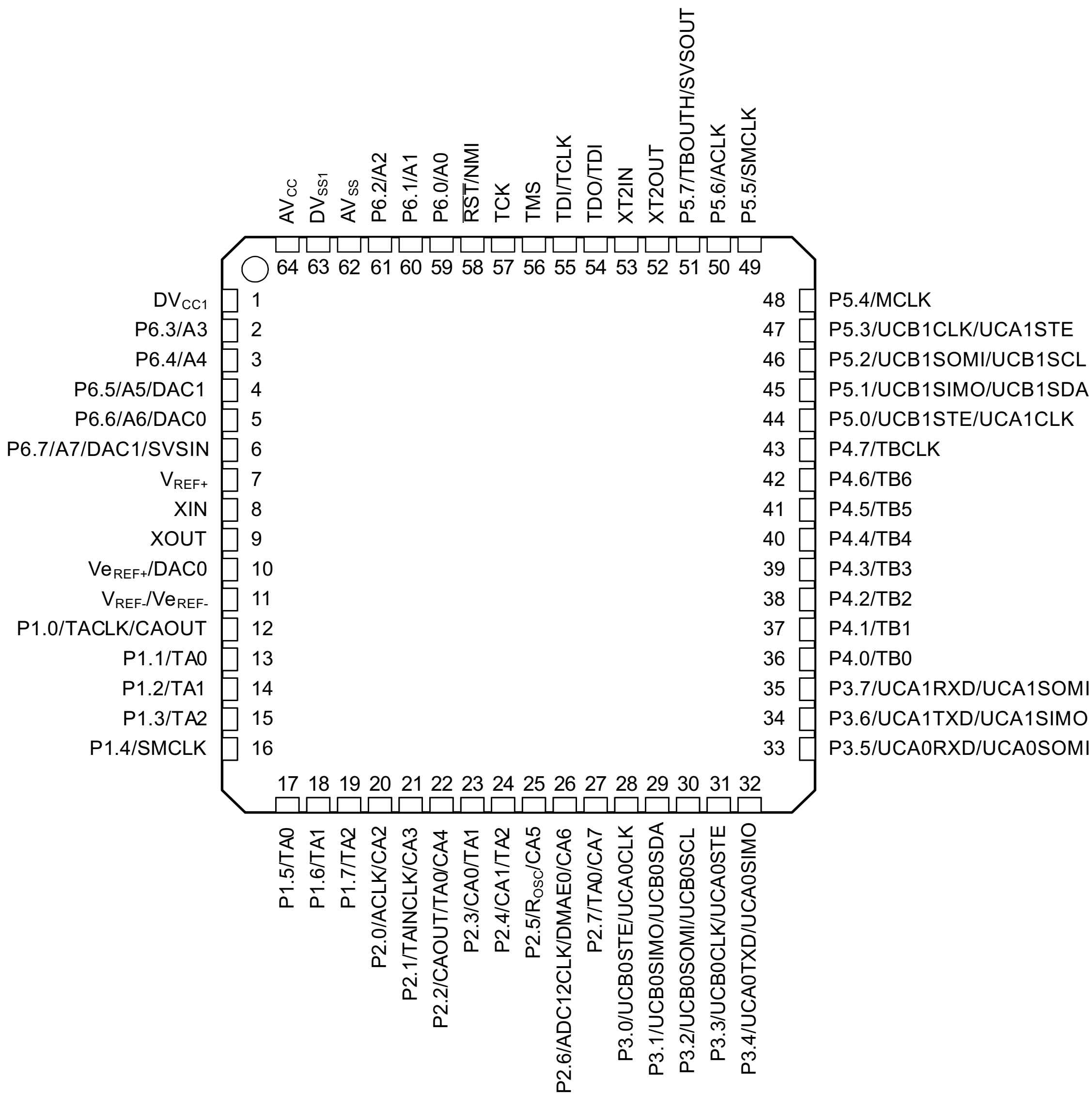


Figure 4-4. 64-Pin PM Package, MSP430F261x (Top View)

Figure 4-5 shows the pinout of the 113-pin ZCA and ZQW packages. For the terminal assignments, see Table 4-1.

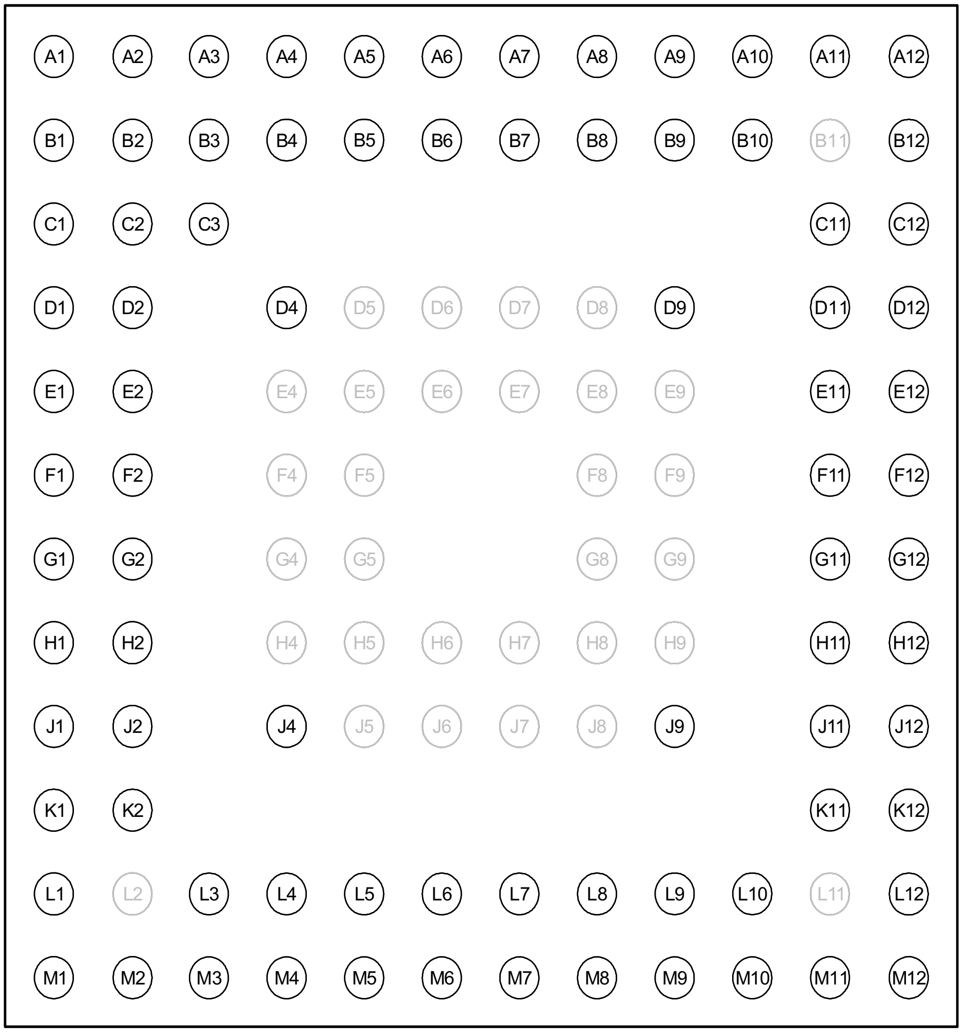


Figure 4-5. 113-Pin ZCA and ZQW Packages (Top View)

4.2 Signal Descriptions

Table 4-1 describes the signals for all device variants and package options.

Table 4-1. Signal Descriptions

TERMINAL				I/O	DESCRIPTION
NAME	NO. PM 64-PIN	NO. PN 80-PIN	NO. ZCA or ZQW 113-PIN		
AV_{CC}	64	80	A2		Analog supply voltage, positive terminal. Supplies only the analog portion of ADC12 and DAC12.
AV_{SS}	62	78	B2, B3		Analog supply voltage, negative terminal. Supplies only the analog portion of ADC12 and DAC12.
DV_{CC1}	1	1	A1		Digital supply voltage, positive terminal. Supplies all digital parts.
DV_{SS1}	63	79	A3		Digital supply voltage, negative terminal. Supplies all digital parts.
DV_{CC2}		52	F12		Digital supply voltage, positive terminal. Supplies all digital parts.
DV_{SS2}		53	E12		Digital supply voltage, negative terminal. Supplies all digital parts.
P1.0/TACLK/CAOUT	12	12	G2	I/O	General-purpose digital I/O pin Timer_A, clock signal TACLK input Comparator_A output
P1.1/TA0	13	13	H1	I/O	General-purpose digital I/O pin Timer_A, capture: CCI0A input, compare: Out0 output BSL transmit
P1.2/TA1	14	14	H2	I/O	General-purpose digital I/O pin Timer_A, capture: CCI1A input, compare: Out1 output
P1.3/TA2	15	15	J1	I/O	General-purpose digital I/O pin Timer_A, capture: CCI2A input, compare: Out2 output
P1.4/SMCLK	16	16	J2	I/O	General-purpose digital I/O pin SMCLK signal output
P1.5/TA0	17	17	K1	I/O	General-purpose digital I/O pin Timer_A, compare: Out0 output
P1.6/TA1	18	18	K2	I/O	General-purpose digital I/O pin Timer_A, compare: Out1 output
P1.7/TA2	19	19	L1	I/O	General-purpose digital I/O pin Timer_A, compare: Out2 output
P2.0/ACLK/CA2	20	20	M1	I/O	General-purpose digital I/O pin ACLK output Comparator_A input
P2.1/TAINCLK/CA3	21	21	M2	I/O	General-purpose digital I/O pin Timer_A, clock signal at INCLK
P2.2/CAOUT/TA0/CA4	22	22	M3	I/O	General-purpose digital I/O pin Timer_A, capture: CCI0B input Comparator_A output BSL receive Comparator_A input
P2.3/CA0/TA1	23	23	L3	I/O	General-purpose digital I/O pin Timer_A, compare: Out1 output Comparator_A input

Table 4-1. Signal Descriptions (continued)

TERMINAL				I/O	DESCRIPTION
NAME	NO. PM 64-PIN	NO. PN 80-PIN	NO. ZCA or ZQW 113-PIN		
P2.4/CA1/TA2	24	24	L4	I/O	General-purpose digital I/O pin Timer_A, compare: Out2 output Comparator_A input
P2.5/R_{OSC}/CA5	25	25	M4	I/O	General-purpose digital I/O pin Input for external resistor defining the DCO nominal frequency Comparator_A input
P2.6/ADC12CLK/ DMAE0[1]/CA6	26	26	J4	I/O	General-purpose digital I/O pin Conversion clock for 12-bit ADC DMA channel 0 external trigger Comparator_A input
P2.7/TA0/CA7	27	27	L5	I/O	General-purpose digital I/O pin Timer_A, compare: Out0 output Comparator_A input
P3.0/UCB0STE/ UCA0CLK	28	28	M5	I/O	General-purpose digital I/O pin USCI_B0 slave transmit enable USCI_A0 clock input/output
P3.1/UCB0SIMO/ UCB0SDA	29	29	L6	I/O	General-purpose digital I/O pin USCI_B0 slave in master out for SPI mode USCI_B0 SDA I^2C data in I^2C mode
P3.2/UCB0SOMI/ UCB0SCL	30	30	M6	I/O	General-purpose digital I/O pin USCI_B0 slave out master in for SPI mode USCI_B0 SCL I^2C clock in I^2C mode
P3.3/UCB0CLK/ UCA0STE	31	31	L7	I/O	General-purpose digital I/O USCI_B0 clock input/output USCI_A0 slave transmit enable
P3.4/UCA0TXD/ UCA0SIMO	32	32	M7	I/O	General-purpose digital I/O pin USCI_A transmit data output in UART mode USCI_A slave data in/master out for SPI mode
P3.5/UCA0RXD/ UCA0SOMI	33	33	L8	I/O	General-purpose digital I/O pin USCI_A0 receive data input in UART mode USCI_A0 slave data out/master in for SPI mode
P3.6/UCA1TXD/ UCA1SIMO	34	34	M8	I/O	General-purpose digital I/O pin USCI_A1 transmit data output in UART mode USCI_A1 slave data in/master out for SPI mode
P3.7/UCA1RXD/ UCA1SOMI	35	35	L9	I/O	General-purpose digital I/O pin USCI_A1 receive data input in UART mode USCI_A1 slave data out/master in for SPI mode
P4.0/TB0	36	36	M9	I/O	General-purpose digital I/O pin Timer_B, capture: CCI0A/B input, compare: Out0 output
P4.1/TB1	37	37	J9	I/O	General-purpose digital I/O pin Timer_B, capture: CCI1A/B input, compare: Out1 output
P4.2/TB2	38	38	M10	I/O	General-purpose digital I/O pin Timer_B, capture: CCI2A/B input, compare: Out2 output

(1) MSP430F261x devices only

Table 4-1. Signal Descriptions (continued)

TERMINAL				I/O	DESCRIPTION
NAME	NO.				
	PM 64-PIN	PN 80-PIN	ZCA or ZQW 113-PIN		
P4.3/TB3	39	39	L10	I/O	General-purpose digital I/O pin Timer_B, capture: CCI3A/B input, compare: Out3 output
P4.4/TB4	40	40	M11	I/O	General-purpose digital I/O pin Timer_B, capture: CCI4A/B input, compare: Out4 output
P4.5/TB5	41	41	M12	I/O	General-purpose digital I/O pin Timer_B, capture: CCI5A/B input, compare: Out5 output
P4.6/TB6	42	42	L12	I/O	General-purpose digital I/O pin Timer_B, capture: CCI6A input, compare: Out6 output
P4.7/TBCLK	43	43	K11	I/O	General-purpose digital I/O pin Timer_B, clock signal TBCLK input
P5.0/UCB1STE/ UCA1CLK	44	44	K12	I/O	General-purpose digital I/O pin USCI_B1 slave transmit enable USCI_A1 clock input/output
P5.1/UCB1SIMO/ UCB1SDA	45	45	J11	I/O	General-purpose digital I/O pin USCI_B1 slave in master out for SPI mode USCI_B1 SDA I^2C data in I^2C mode
P5.2/UCB1SOMI/ UCB1SCL	46	46	J12	I/O	General-purpose digital I/O pin USCI_B1 slave out master in for SPI mode USCI_B1 SCL I^2C clock in I^2C mode
P5.3/UCB1CLK/ UCA1STE	47	47	H11	I/O	General-purpose digital I/O USCI_B1 clock input/output USCI_A1 slave transmit enable
P5.4/MCLK	48	48	H12	I/O	General-purpose digital I/O pin Main system clock MCLK output
P5.5/SMCLK	49	49	G11	I/O	General-purpose digital I/O pin Submain system clock SMCLK output
P5.6/ACLK	50	50	G12	I/O	General-purpose digital I/O pin Auxiliary clock ACLK output
P5.7/TBOUTH/SVSOUT	51	51	F11	I/O	General-purpose digital I/O pin Switch all PWM digital output ports to high impedance – Timer_B TB0 to TB6 SVS comparator output
P6.0/A0	59	75	D4	I/O	General-purpose digital I/O pin Analog input A0 for 12-bit ADC
P6.1/A1	60	76	A4	I/O	General-purpose digital I/O pin Analog input A1 for 12-bit ADC
P6.2/A2	61	77	B4	I/O	General-purpose digital I/O pin Analog input A2 for 12-bit ADC
P6.3/A3	2	2	B1	I/O	General-purpose digital I/O pin Analog input A3 for 12-bit ADC
P6.4/A4	3	3	C1	I/O	General-purpose digital I/O pin Analog input A4 for 12-bit ADC

Table 4-1. Signal Descriptions (continued)

TERMINAL				I/O	DESCRIPTION
NAME	NO.				
	PM 64-PIN	PN 80-PIN	ZCA or ZQW 113-PIN		
P6.5/A5/DAC1 (1)	4	4	C2, C3	I/O	General-purpose digital I/O pin Analog input A5 for 12-bit ADC DAC12.1 output
P6.6/A6/DAC0 (1)	5	5	D1	I/O	General-purpose digital I/O pin Analog input A6 for 12-bit ADC DAC12.0 output
P6.7/A7/DAC1 (1)/SVSIN	6	6	D2	I/O	General-purpose digital I/O pin Analog input A7 for 12-bit ADC DAC12.1 output SVS input
P7.0		54	E11	I/O	General-purpose digital I/O pin
P7.1		55	D12	I/O	General-purpose digital I/O pin
P7.2		56	D11	I/O	General-purpose digital I/O pin
P7.3		57	C12	I/O	General-purpose digital I/O pin
P7.4		58	C11	I/O	General-purpose digital I/O pin
P7.5		59	B12	I/O	General-purpose digital I/O pin
P7.6		60	A12	I/O	General-purpose digital I/O pin
P7.7		61	A11	I/O	General-purpose digital I/O pin
P8.0		62	B10	I/O	General-purpose digital I/O pin
P8.1		63	A10	I/O	General-purpose digital I/O pin
P8.2		64	D9	I/O	General-purpose digital I/O pin
P8.3		65	A9	I/O	General-purpose digital I/O pin
P8.4		66	B9	I/O	General-purpose digital I/O pin
P8.5		67	B8	I/O	General-purpose digital I/O pin
P8.6/XT2OUT		68	A8	I/O	General-purpose digital I/O pin Output terminal of crystal oscillator XT2
P8.7/XT2IN		69	A7	I/O	General-purpose digital I/O pin Input port for crystal oscillator XT2. Only standard crystals can be connected.
XT2OUT	52			O	Output terminal of crystal oscillator XT2
XT2IN	53			I	Input port for crystal oscillator XT2
RST/NMI	58	74	B5	I	Reset input, nonmaskable interrupt input port, or bootloader start (in flash devices)
TCK	57	73	A5	I	Test clock (JTAG). TCK is the clock input port for device programming test and bootloader start
TDI/TCLK	55	71	A6	I	Test data input or test clock input. The device protection fuse is connected to TDI/TCLK.
TDO/TDI	54	70	B7	I/O	Test data output port. TDO/TDI data output or programming data input terminal.
TMS	56	72	B6	I	Test mode select. TMS is used as an input port for device programming and test.
V_{eREF+}/DAC0 (1)	10	10	F2	I	Input for an external reference voltage DAC12.0 output
V_{REF+}	7	7	E2	O	Output of positive terminal of the reference voltage in the ADC12
V_{REF-}/V_{eREF-}	11	11	G1	I	Negative terminal for the reference voltage for both sources, the internal reference voltage or an external applied reference voltage

Table 4-1. Signal Descriptions (continued)

TERMINAL				I/O	DESCRIPTION
NAME	NO.				
	PM 64-PIN	PN 80-PIN	ZCA or ZQW 113-PIN		
XIN	8	8	E1	I	Input port for crystal oscillator XT1. Standard or watch crystals can be connected.
XOUT	9	9	F1	O	Output port for crystal oscillator XT1. Standard or watch crystals can be connected.
Reserved	–	–	(2)	NA	Reserved pins. TI recommends connecting to DV_{SS} and AV_{SS}.

(2) Reserved pins are L2, E4, F4, G4, H4, D5, E5, F5, G5, H5, J5, D6, E6, H6, J6, D7, E7, H7, J7, D8, E8, F8, G8, H8, J8, E9, F9, G9, H9, B11, L11.

5 Specifications

5.1 Absolute Maximum Ratings[(1)]

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
Voltage applied at V_{CC} to V_{SS}		–0.3	4.1	V
Voltage applied to any pin[(2)]		–0.3	V_{CC} + 0.3	V
Diode current at any device terminal		–2	2	mA
Storage temperature, T_{stg}[(3)]	Unprogrammed device	–55	150	°C
	Programmed device	–55	150	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages referenced to V_{SS}. The JTAG fuse-blow voltage, V_{FB}, is allowed to exceed the absolute maximum rating. The voltage is applied to the TEST pin when blowing the JTAG fuse.
(3) Higher temperature may be applied during board soldering according to the current JEDEC J-STD-020 specification with peak reflow temperatures not higher than classified on the device label on the shipping boxes or reels.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[(1)]	±1000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101[(2)]	±250	

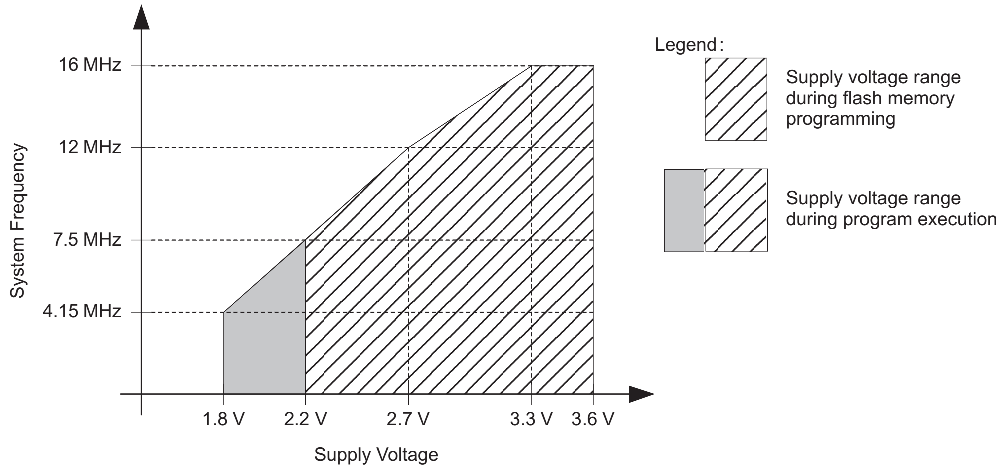
(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Pins listed as ±1000 V may actually have higher performance.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Pins listed as ±250 V may actually have higher performance.

5.3 Recommended Operating Conditions

Typical values are specified at V_{CC} = 3.3 V and T_A = 25°C (unless otherwise noted)

			MIN	MAX	UNIT
V_{CC}	Supply voltage (AV_{CC} = DV_{CC} = V_{CC}[(1)])	During program execution	1.8	3.6	V
		During flash program or erase	2.2	3.6	
V_{SS}	Supply voltage (AV_{SS} = DV_{SS} = V_{SS})		0	0	V
T_A	Operating free-air temperature	T version	–40	105	°C
f_{SYSTEM}	Processor frequency (maximum MCLK frequency)[(2)(3)] (see Figure 5-1)	V_{CC} = 1.8 V, Duty cycle = 50% ±10%	DC	4.15	MHz
		V_{CC} = 2.7 V, Duty cycle = 50% ±10%	DC	12	
		V_{CC} ≥ 3.3 V, Duty cycle = 50% ±10%	DC	16	

(1) TI recommends powering AV_{CC} and DV_{CC} from the same source. A maximum difference of 0.3 V between AV_{CC} and DV_{CC} can be tolerated during power up.
(2) The MSP430 CPU is clocked directly with MCLK. Both the high and low phases of MCLK must not exceed the pulse duration of the specified maximum frequency.
(3) Modules might have a different maximum input clock specification. See the specification of the respective module in this data sheet.



Note: Minimum processor frequency is defined by system clock. Flash program or erase operations require a minimum V_{CC} of 2.2 V.

Figure 5-1. Operating Area

5.4 Active Mode Supply Current Into V_{CC} Excluding External Current

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)(1)(2) (see Figure 5-2 and Figure 5-3)

PARAMETER		TEST CONDITIONS	T_A	V_{CC}	MIN	TYP	MAX	UNIT
$I_{AM,1MHz}$	Active mode (AM) current (1 MHz)	$f_{DCO} = f_{MCLK} = f_{SMCLK}$ = 1 MHz, f_{ACLK} = 32768 Hz, Program executes in flash, BCSCTL1 = CALBC1_1MHZ, DCOCTL = CALDCO_1MHZ, CPUOFF = 0, SCG0 = 0, SCG1 = 0, OSCOFF = 0	–40°C to 85°C	2.2 V		365	395	µA
			105°C	2.2 V		375	420	
			–40°C to 85°C	3 V		515	560	
			105°C	3 V		525	595	
$I_{AM,1MHz}$	Active mode (AM) current (1 MHz)	$f_{DCO} = f_{MCLK} = f_{SMCLK}$ = 1 MHz, f_{ACLK} = 32768 Hz, Program executes in RAM, BCSCTL1 = CALBC1_1MHZ, DCOCTL = CALDCO_1MHZ, CPUOFF = 0, SCG0 = 0, SCG1 = 0, OSCOFF = 0	–40°C to 85°C	2.2 V		330	370	µA
			105°C	2.2 V		340	390	
			–40°C to 85°C	3 V		460	495	
			105°C	3 V		470	520	
$I_{AM,4kHz}$	Active mode (AM) current (4 kHz)	$f_{MCLK} = f_{SMCLK} = f_{ACLK}$ = 32768 Hz/8 = 4096 Hz, f_{DCO} = 0 Hz, Program executes in flash, SELMx = 11, SELS = 1, DIVMx = DIVSx = DIVAx = 11, CPUOFF = 0, SCG0 = 1, SCG1 = 0, OSCOFF = 0	–40°C to 85°C	2.2 V		2.1	9	µA
			105°C	2.2 V		15	31	
			–40°C to 85°C	3 V		3	11	
			105°C	3 V		19	32	
$I_{AM,100kHz}$	Active mode (AM) current (100 kHz)	$f_{MCLK} = f_{SMCLK} = f_{DCO(0, 0)} \approx$ 100 kHz, f_{ACLK} = 0 Hz, Program executes in flash, RSELx = 0, DCOx = 0, CPUOFF = 0, SCG0 = 0, SCG1 = 0, OSCOFF = 1	–40°C to 85°C	2.2 V		67	86	µA
			105°C	2.2 V		80	99	
			–40°C to 85°C	3 V		84	107	
			105°C	3 V		99	128	

(1) All inputs are tied to 0 V or to V_{CC}. Outputs do not source or sink any current.
(2) The currents are characterized with a Micro Crystal CC4V-T1A SMD crystal with a load capacitance of 9 pF. The internal and external load capacitance is chosen to closely match the required 9 pF.

5.5 Typical Characteristics – Active Mode Supply Current (Into V_{CC})

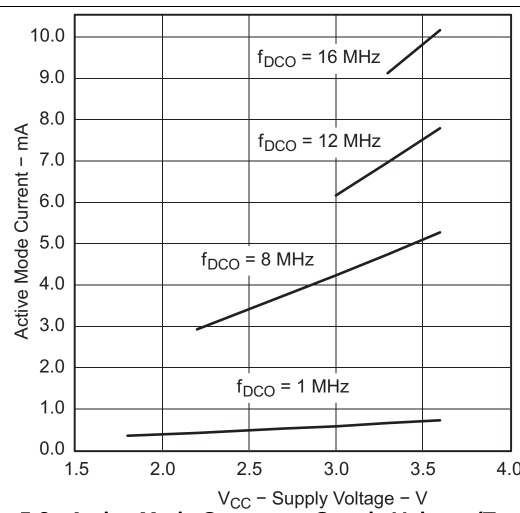


Figure 5-2. Active Mode Current vs Supply Voltage (T_A = 25°C)

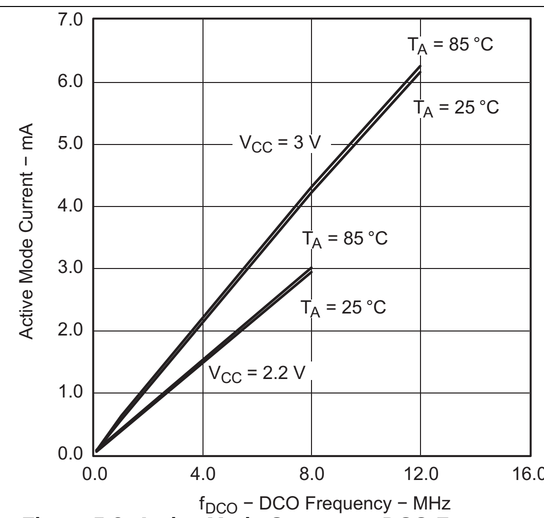


Figure 5-3. Active Mode Current vs DCO Frequency

5.6 Low-Power Mode Supply Currents (Into V_{CC}) Excluding External Current

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)(1) (2)

PARAMETER		TEST CONDITIONS	T_A	V_{CC}	MIN	TYP	MAX	UNIT
$I_{LPM0,1MHz}$	Low-power mode 0 (LPM0) current(3)	f_{MCLK} = 0 MHz, f_{SMCLK} = f_{DCO} = 1 MHz, f_{ACLK} = 32,768 Hz, BCSCTL1 = CALBC1_1MHZ, DCOCTL = CALDCO_1MHZ, CPUOFF = 1, SCG0 = 0, SCG1 = 0, OSCOFF = 0	–40°C to 85°C	2.2 V		68	63	µA
			105°C			83	98	
			–40°C to 85°C	3 V		87	105	
			105°C			100	125	
$I_{LPM0,100kHz}$	Low-power mode 0 (LPM0) current(3)	f_{MCLK} = 0 MHz, f_{SMCLK} = $f_{DCO(0, 0)}$ ≈ 100 kHz, f_{ACLK} = 0 Hz, RSELx = 0, DCOx = 0, CPUOFF = 1, SCG0 = 0, SCG1 = 0, OSCOFF = 1	–40°C to 85°C	2.2 V		37	49	µA
			105°C			50	62	
			–40°C to 85°C	3 V		40	55	
			105°C			57	73	
I_{LPM2}	Low-power mode 2 (LPM2) current(4)	f_{MCLK} = f_{SMCLK} = 0 MHz, f_{DCO} = 1 MHz, f_{ACLK} = 32,768 Hz, BCSCTL1 = CALBC1_1MHZ, DCOCTL = CALDCO_1MHZ, CPUOFF = 1, SCG0 = 0, SCG1 = 1, OSCOFF = 0	–40°C to 85°C	2.2 V		23	33	µA
			105°C			35	46	
			–40°C to 85°C	3 V		25	36	
			105°C			40	55	
$I_{LPM3,LFXT1}$	Low-power mode 3 (LPM3) current(3)	f_{DCO} = f_{MCLK} = f_{SMCLK} = 0 MHz, f_{ACLK} = 32,768 Hz, CPUOFF = 1, SCG0 = 1, SCG1 = 1, OSCOFF = 0	–40°C	2.2 V		0.8	1.2	µA
			25°C			1	1.3	
			85°C			4.6	7	
			105°C			14	24	
			–40°C	3 V		0.9	1.3	
			25°C			1.1	1.5	
			85°C			5.5	8	
			105°C			17	30	
$I_{LPM3,VLO}$	Low-power mode 3 (LPM3) current(4)	f_{DCO} = f_{MCLK} = f_{SMCLK} = 0 MHz, f_{ACLK} from internal LF oscillator (VLO), CPUOFF = 1, SCG0 = 1, SCG1 = 1, OSCOFF = 0	–40°C	2.2 V		0.4	1	µA
			25°C			0.5	1	
			85°C			4.3	6.5	
			105°C			14	24	
			–40°C	3 V		0.6	1.2	
			25°C			0.6	1.2	
			85°C			5	7.5	
			105°C			16.5	29.5	
I_{LPM4}	Low-power mode 4 (LPM4) current(5) (see Figure 5-4)	f_{DCO} = f_{MCLK} = f_{SMCLK} = 0 MHz, f_{ACLK} = 0 Hz, CPUOFF = 1, SCG0 = 1, SCG1 = 1, OSCOFF = 1	–40°C	2.2 V		0.1	0.5	µA
			25°C			0.1	0.5	
			85°C			4	6	
			105°C			13	23	
			–40°C	3 V		0.2	0.5	
			25°C			0.2	0.5	
			85°C			4.7	7	
			105°C			14	24	

(1) All inputs are tied to 0 V or to V_{CC}. Outputs do not source or sink any current.
(2) The currents are characterized with a Micro Crystal CC4V-T1A SMD crystal with a load capacitance of 9 pF.
(3) Current for brownout and WDT clocked by SMCLK included.
(4) Current for brownout and WDT clocked by ACLK included.
(5) Current for brownout included.

5.7 Typical Characteristics – LPM4 Current

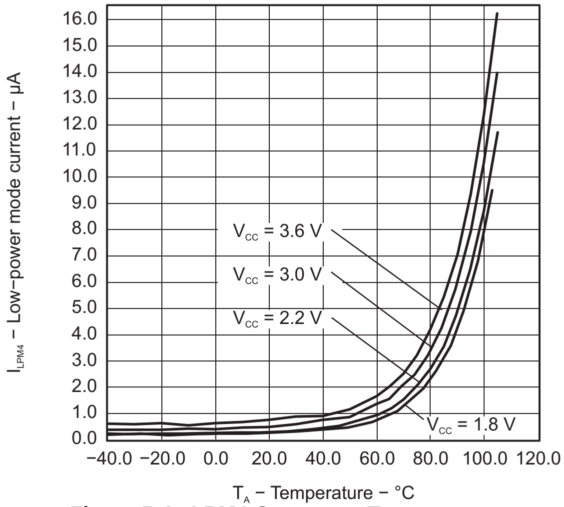


Figure 5-4. LPM4 Current vs Temperature

5.8 Schmitt-Trigger Inputs (Ports P1 to P8, $\overline{RST}$/NMI, JTAG, XIN, and XT2IN)(1)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
V_{IT+}	Positive-going input threshold voltage			0.45 V_{CC}		0.75 V_{CC}	V
			2.2 V	1.00		1.65	
			3 V	1.35		2.25	
V_{IT-}	Negative-going input threshold voltage			0.25 V_{CC}		0.55 V_{CC}	V
			2.2 V	0.55		1.20	
			3 V	0.75		1.65	
V_{hys}	Input voltage hysteresis (V_{IT+} – V_{IT-})		2.2 V	0.2		1	V
			3 V	0.3		1	
R_{Pull}	Pullup/pulldown resistor	For pullup: V_{IN} = V_{SS}, For pulldown: V_{IN} = V_{CC}		20	35	50	kΩ
C_I	Input capacitance	V_{IN} = V_{SS} or V_{CC}			5		pF

(1) XIN and XT2IN in bypass mode only

5.9 Inputs (Ports P1 and P2)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	MAX	UNIT
$t_{(int)}$	External interrupt timing	Port P1, P2: P1.x to P2.x, External trigger pulse duration to set interrupt flag(1)	2.2 V, 3 V	20		ns

(1) An external signal sets the interrupt flag every time the minimum interrupt pulse duration $t_{(int)}$ is met. It may be set even with trigger signals shorter than $t_{(int)}$.

5.10 Leakage Current (Ports P1 to P8)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		V_{CC}	MIN	MAX	UNIT
$I_{lkg(Px.y)}$	High-impedance leakage current(1) (2)	2.2 V, 3 V		±50	nA

(1) The leakage current is measured with V_{SS} or V_{CC} applied to the corresponding pins, unless otherwise noted.
(2) The leakage of the digital port pins is measured individually. The port pin is selected for input and the pullup or pulldown resistor is disabled.

5.11 Standard Inputs ($\overline{RST}$/NMI)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		V_{CC}	MIN	MAX	UNIT
V_{IL}	Low-level input voltage	2.2 V, 3 V	V_{SS}	V_{SS} + 0.6	V
V_{IH}	High-level input voltage	2.2 V, 3 V	0.8 V_{CC}	V_{CC}	V

5.12 Outputs (Ports P1 to P8)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)
(also see Figure 5-5, Figure 5-6, Figure 5-7, and Figure 5-8)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	$I_{(OHmax)}$ = –1.5 mA (1)	2.2 V	V_{CC} – 0.25		V_{CC}	V
		$I_{(OHmax)}$ = –6 mA (2)	2.2 V	V_{CC} – 0.6		V_{CC}	
		$I_{(OHmax)}$ = –1.5 mA (1)	3 V	V_{CC} – 0.25		V_{CC}	
		$I_{(OHmax)}$ = –6 mA (2)	3 V	V_{CC} – 0.6		V_{CC}	
V_{OL}	Low-level output voltage	$I_{(OLmax)}$ = 1.5 mA (1)	2.2 V	V_{SS}		V_{SS} + 0.25	V
		$I_{(OLmax)}$ = 6 mA (2)	2.2 V	V_{SS}		V_{SS} + 0.6	
		$I_{(OLmax)}$ = 1.5 mA (1)	3 V	V_{SS}		V_{SS} + 0.25	
		$I_{(OLmax)}$ = 6 mA (2)	3 V	V_{SS}		V_{SS} + 0.6	

(1) The maximum total current, $I_{(OHmax)}$ and $I_{(OLmax)}$, for all outputs combined should not exceed ±12 mA to hold the maximum voltage drop specified.
(2) The maximum total current, $I_{(OHmax)}$ and $I_{(OLmax)}$, for all outputs combined should not exceed ±48 mA to hold the maximum voltage drop specified.

5.13 Output Frequency (Ports P1 to P8)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$f_{Px.y}$	Port output frequency (with load)	P1.4/SMCLK, C_L = 20 pF, R_L = 1 kΩ (1) (2)	2.2 V	DC		10	MHz
			3 V	DC		12	
$f_{Port°CLK}$	Clock output frequency	P2.0/ACLK/CA2, P1.4/SMCLK, C_L = 20 pF (2)	2.2 V	DC		12	MHz
			3 V	DC		16	
$t_{(Xdc)}$	Duty cycle of output frequency	P5.6/ACLK, C_L = 20 pF, LF mode		30%	50%	70%	
		P5.6/ACLK, C_L = 20 pF, XT1 mode		40%	50%	60%	
		P5.4/MCLK, C_L = 20 pF, XT1 mode		40%		60%	
		P5.4/MCLK, C_L = 20 pF, DCO		50% – 15 ns		50% + 15 ns	
		P1.4/SMCLK, C_L = 20 pF, XT2 mode		40%		60%	
		P1.4/SMCLK, C_L = 20 pF, DCO		50% – 15 ns		50% + 15 ns	

(1) A resistive divider with two 0.5-kΩ resistors between V_{CC} and V_{SS} is used as load. The output is connected to the center tap of the divider.
(2) The output voltage reaches at least 10% and 90% V_{CC} at the specified toggle frequency.

5.14 Typical Characteristics – Outputs

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

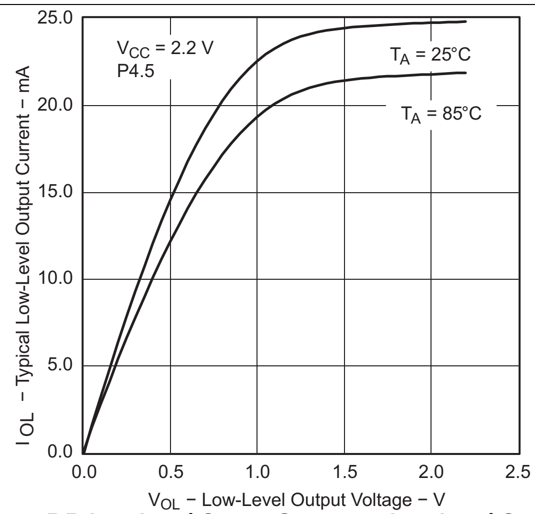


Figure 5-5. Low-Level Output Current vs Low-Level Output Voltage

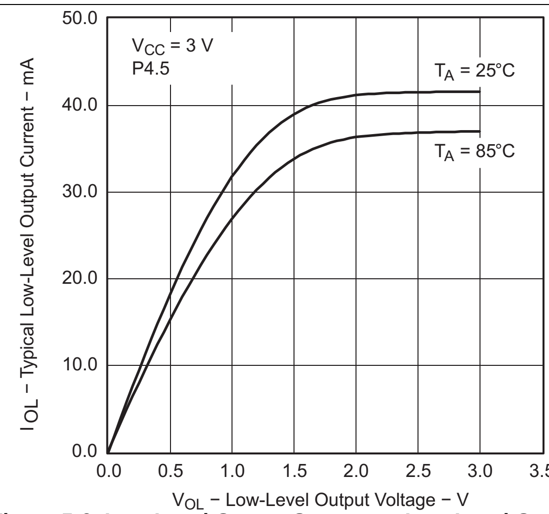


Figure 5-6. Low-Level Output Current vs Low-Level Output Voltage

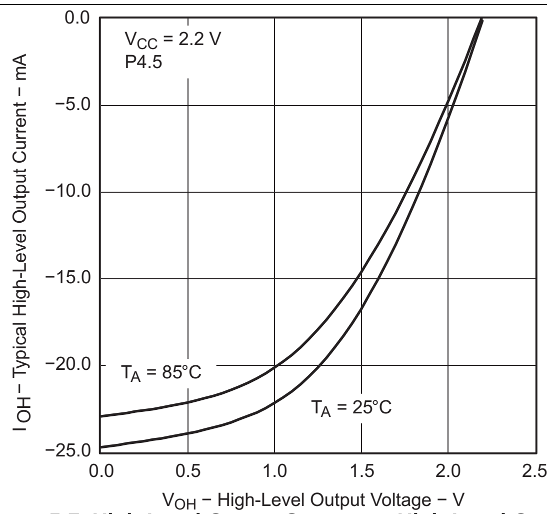


Figure 5-7. High-Level Output Current vs High-Level Output Voltage

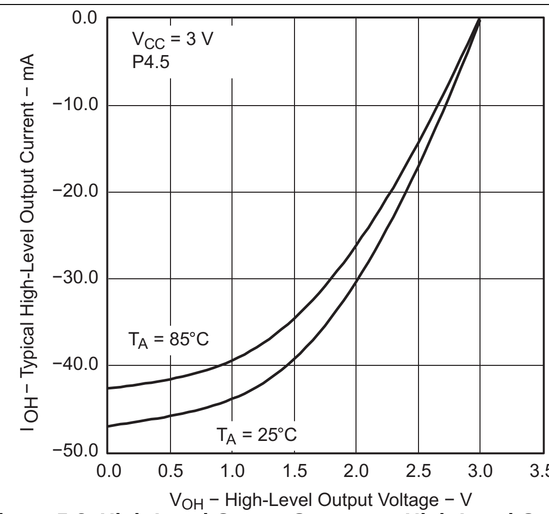


Figure 5-8. High-Level Output Current vs High-Level Output Voltage

5.15 POR and Brownout Reset (BOR)(1)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$V_{CC(start)}$	See Figure 5-9	$dV_{CC}/dt \le 3$ V/s			0.7 × $V_{(B\_IT-)}$		V
$V_{(B\_IT-)}$	See Figure 5-9, Figure 5-10, and Figure 5-11	$dV_{CC}/dt \le 3$ V/s				1.71	V
$V_{hys(B\_IT-)}$	See Figure 5-9	$dV_{CC}/dt \le 3$ V/s		70	130	210	mV
$t_{d(BOR)}$	See Figure 5-9					2000	µs
$t_{(reset)}$	Pulse duration needed at $\overline{\text{RST}}$/NMI pin to accept reset internally		2.2 V, 3 V	2			µs

(1) The current consumption of the brownout module is already included in the I_{CC} current consumption data. The voltage level $V_{(B\_IT-)} + V_{hys(B\_IT-)}$ is ≤ 1.8 V.

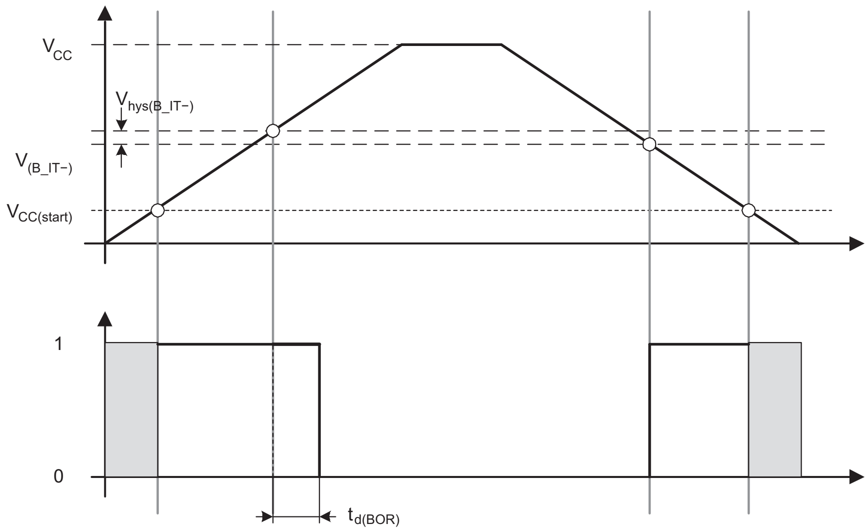


Figure 5-9. POR and BOR vs Supply Voltage

5.16 Typical Characteristics – POR and BOR

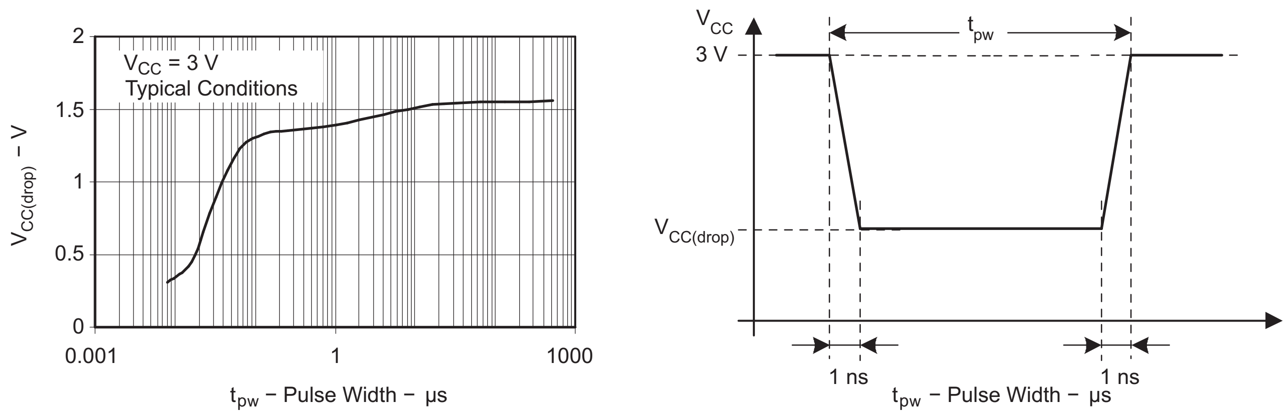


Figure 5-10. $V_{CC(drop)}$ Level With a Rectangular Voltage Drop to Generate a POR or BOR Signal

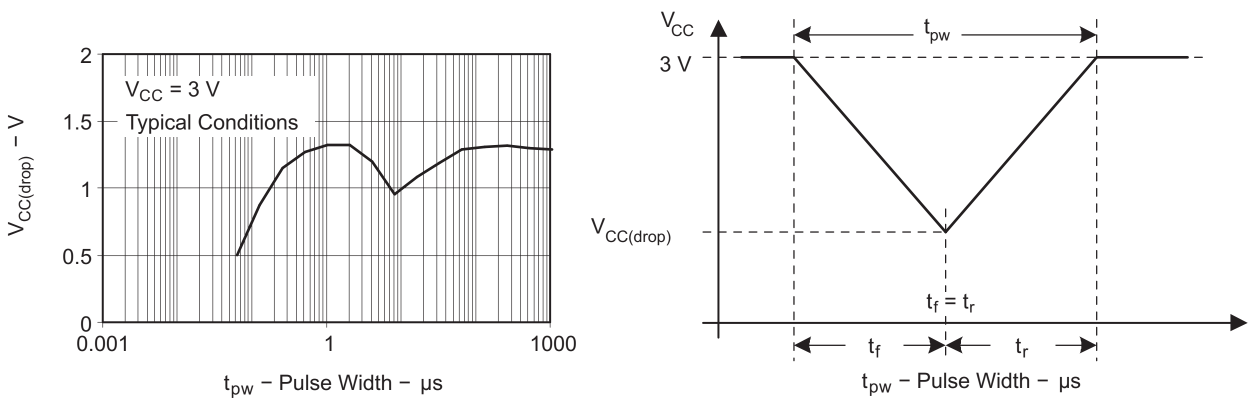


Figure 5-11. $V_{CC(drop)}$ Level With a Triangular Voltage Drop to Generate a POR or BOR Signal

5.17 Supply Voltage Supervisor (SVS), Supply Voltage Monitor (SVM)

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
$t_{(SVSR)}$	$dV_{CC}/dt > 30$ V/ms (see Figure 5-12)		5		150	µs
	$dV_{CC}/dt \le 30$ V/ms				2000	
$t_{d(SVSon)}$	SVSon, switch from VLD = 0 to VLD ≠ 0, V_{CC} = 3 V			150	300	µs
t_{settle}	VLD ≠ 0 (1)				12	µs
$V_{(SVSstart)}$	VLD ≠ 0, $V_{CC}/dt \le 3$ V/s (see Figure 5-12)			1.55	1.7	V
$V_{hys(SVS\_IT-)}$	$V_{CC}/dt \le 3$ V/s (see Figure 5-12)	VLD = 1	70	120	155	mV
		VLD = 2 to 14	0.004 × $V_{(SVS\_IT-)}$		0.016 × $V_{(SVS\_IT-)}$	V
	$V_{CC}/dt \le 3$ V/s (see Figure 5-12), external voltage applied on A7	VLD = 15	4.4		20	mV
$V_{(SVS\_IT-)}$	$V_{CC}/dt \le 3$ V/s (see Figure 5-12 and Figure 5-13)	VLD = 1	1.8	1.9	2.05	V
		VLD = 2	1.94	2.1	2.25	
		VLD = 3	2.05	2.2	2.37	
		VLD = 4	2.14	2.3	2.48	
		VLD = 5	2.24	2.4	2.60	
		VLD = 6	2.33	2.5	2.71	
		VLD = 7	2.46	2.65	2.86	
		VLD = 8	2.58	2.8	3	
		VLD = 9	2.69	2.9	3.13	
		VLD = 10	2.83	3.05	3.29	
		VLD = 11	2.94	3.2	3.42	
		VLD = 12	3.11	3.35	3.61 (2)	
		VLD = 13	3.24	3.5	3.76 (2)	
		VLD = 14	3.43	3.7 (2)	3.99 (2)	
	$V_{CC}/dt \le 3$ V/s (see Figure 5-12 and Figure 5-13), external voltage applied on A7	VLD = 15	1.1	1.2	1.3	
$I_{CC(SVS)}$ (3)	VLD ≠ 0, V_{CC} = 2.2 V, 3 V			10	15	µA

(1) t_{settle} is the settling time that the comparator output requires to have a stable level after VLD is switched from VLD ≠ 0 to a different VLD value somewhere between 2 and 15. The overdrive is assumed to be >50 mV.
(2) The recommended operating voltage range is limited to 3.6 V.
(3) The current consumption of the SVS module is not included in the I_{CC} current consumption data.

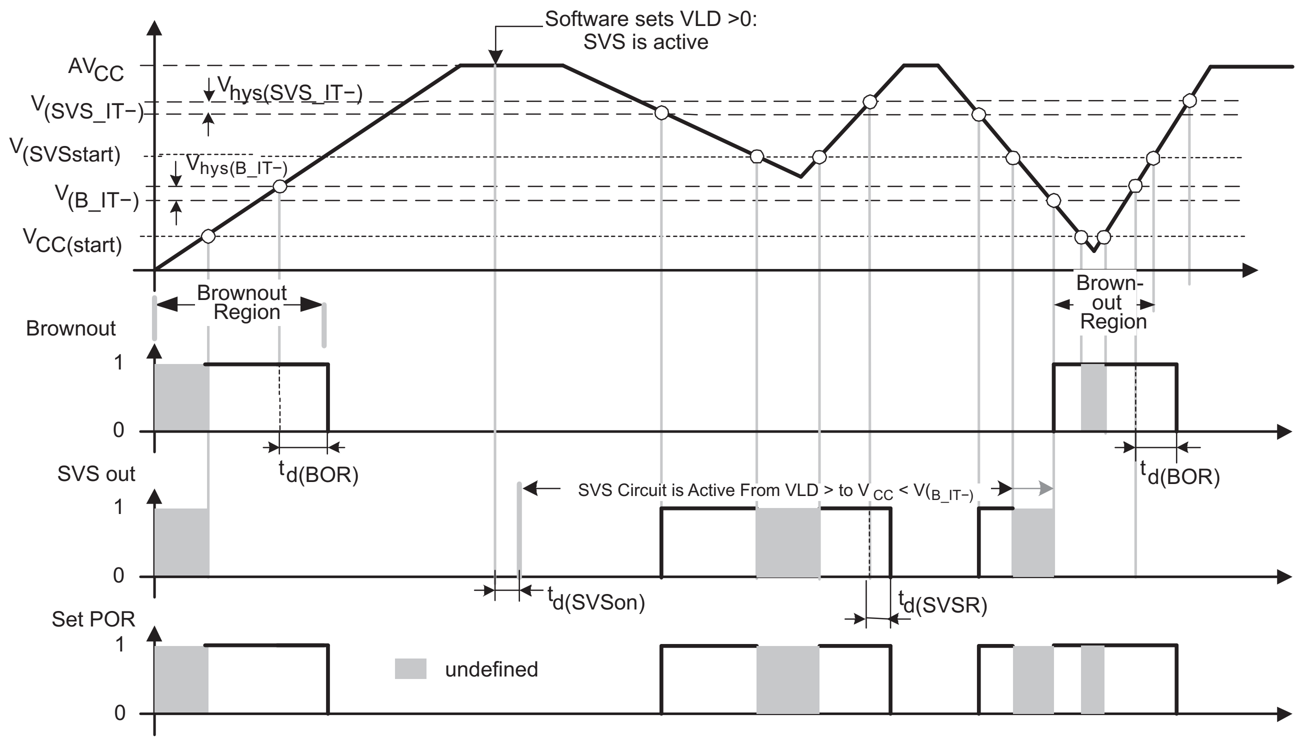


Figure 5-12. SVS Reset (SVSR) vs Supply Voltage

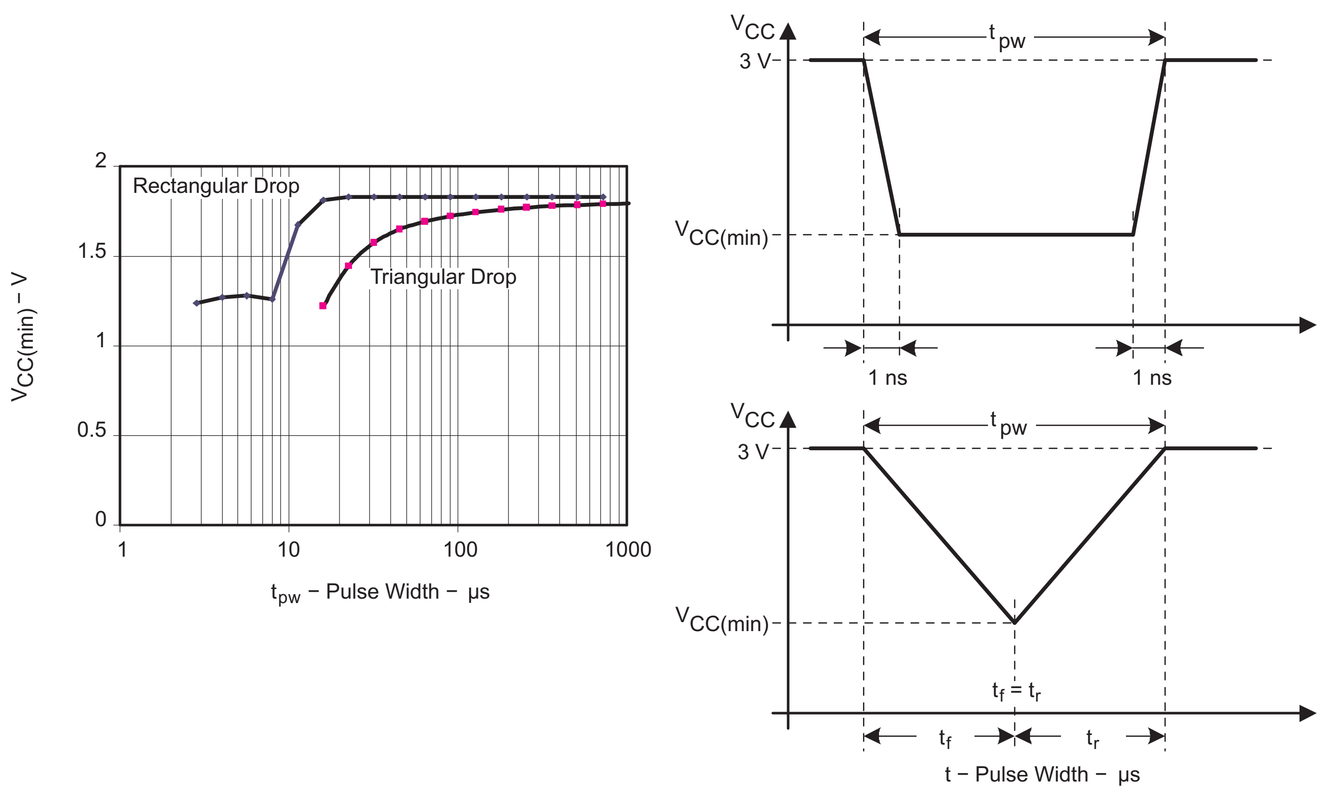


Figure 5-13. $V_{CC(min)}$: Rectangular Voltage Drop and Triangular Voltage Drop to Generate an SVS Signal (VLD = 1)

5.18 Main DCO Characteristics

- All ranges selected by RSELx overlap with RSELx + 1: RSELx = 0 overlaps RSELx = 1, ... RSELx = 14 overlaps RSELx = 15.
- DCO control bits DCOx have a step size as defined by parameter S_{DCO}.
- Modulation control bits MODx select how often $f_{DCO(RSEL,DCO+1)}$ is used within the period of 32 DCOCLK cycles. The frequency $f_{DCO(RSEL,DCO)}$ is used for the remaining cycles. The frequency is an average equal to:

$$f_{average} = \frac{32 \times f_{DCO(RSEL,DCO)} \times f_{DCO(RSEL,DCO+1)}}{MOD \times f_{DCO(RSEL,DCO)} + (32 - MOD) \times f_{DCO(RSEL,DCO+1)}}$$

5.19 DCO Frequency

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
V_{CC}	Supply voltage	RSELx < 14		1.8		3.6	V
		RSELx = 14		2.2		3.6	
		RSELx = 15		3.0		3.6	
$f_{DCO(0,0)}$	DCO frequency (0, 0)	RSELx = 0, DCOx = 0, MODx = 0	2.2 V, 3 V	0.06		0.14	MHz
$f_{DCO(0,3)}$	DCO frequency (0, 3)	RSELx = 0, DCOx = 3, MODx = 0	2.2 V, 3 V	0.07		0.17	MHz
$f_{DCO(1,3)}$	DCO frequency (1, 3)	RSELx = 1, DCOx = 3, MODx = 0	2.2 V, 3 V	0.10		0.20	MHz
$f_{DCO(2,3)}$	DCO frequency (2, 3)	RSELx = 2, DCOx = 3, MODx = 0	2.2 V, 3 V	0.14		0.28	MHz
$f_{DCO(3,3)}$	DCO frequency (3, 3)	RSELx = 3, DCOx = 3, MODx = 0	2.2 V, 3 V	0.20		0.40	MHz
$f_{DCO(4,3)}$	DCO frequency (4, 3)	RSELx = 4, DCOx = 3, MODx = 0	2.2 V, 3 V	0.28		0.54	MHz
$f_{DCO(5,3)}$	DCO frequency (5, 3)	RSELx = 5, DCOx = 3, MODx = 0	2.2 V, 3 V	0.39		0.77	MHz
$f_{DCO(6,3)}$	DCO frequency (6, 3)	RSELx = 6, DCOx = 3, MODx = 0	2.2 V, 3 V	0.54		1.06	MHz
$f_{DCO(7,3)}$	DCO frequency (7, 3)	RSELx = 7, DCOx = 3, MODx = 0	2.2 V, 3 V	0.80		1.50	MHz
$f_{DCO(8,3)}$	DCO frequency (8, 3)	RSELx = 8, DCOx = 3, MODx = 0	2.2 V, 3 V	1.10		2.10	MHz
$f_{DCO(9,3)}$	DCO frequency (9, 3)	RSELx = 9, DCOx = 3, MODx = 0	2.2 V, 3 V	1.60		3.00	MHz
$f_{DCO(10,3)}$	DCO frequency (10, 3)	RSELx = 10, DCOx = 3, MODx = 0	2.2 V, 3 V	2.50		4.30	MHz
$f_{DCO(11,3)}$	DCO frequency (11, 3)	RSELx = 11, DCOx = 3, MODx = 0	2.2 V, 3 V	3.00		5.50	MHz
$f_{DCO(12,3)}$	DCO frequency (12, 3)	RSELx = 12, DCOx = 3, MODx = 0	2.2 V, 3 V	4.30		7.30	MHz
$f_{DCO(13,3)}$	DCO frequency (13, 3)	RSELx = 13, DCOx = 3, MODx = 0	2.2 V, 3 V	6.00		9.60	MHz
$f_{DCO(14,3)}$	DCO frequency (14, 3)	RSELx = 14, DCOx = 3, MODx = 0	2.2 V, 3 V	8.60		13.9	MHz
$f_{DCO(15,3)}$	DCO frequency (15, 3)	RSELx = 15, DCOx = 3, MODx = 0	3 V	12.0		18.5	MHz
$f_{DCO(15,7)}$	DCO frequency (15, 7)	RSELx = 15, DCOx = 7, MODx = 0	3 V	16.0		26.0	MHz
S_{RSEL}	Frequency step between range RSEL and RSEL+1	$S_{RSEL} = f_{DCO(RSEL+1,DCO)}/f_{DCO(RSEL,DCO)}$	2.2 V, 3 V			1.55	ratio
S_{DCO}	Frequency step between tap DCO and DCO+1	$S_{DCO} = f_{DCO(RSEL,DCO+1)}/f_{DCO(RSEL,DCO)}$	2.2 V, 3 V	1.05	1.08	1.12	ratio
	Duty cycle	Measured at P1.4/SMCLK	2.2 V, 3 V	40%	50%	60%	

5.20 Calibrated DCO Frequencies – Tolerance at Calibration

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	V_{CC}	MIN	TYP	MAX	UNIT
	Frequency tolerance at calibration		25°C	3 V	–1%	±0.2%	+1%	
$f_{CAL(1MHz)}$	1-MHz calibration value	BCSCTL1 = CALBC1_1MHZ, DCOCTL = CALDCO_1MHZ, Gating time: 5 ms	25°C	3 V	0.990	1	1.010	MHz
$f_{CAL(8MHz)}$	8-MHz calibration value	BCSCTL1 = CALBC1_8MHZ, DCOCTL = CALDCO_8MHZ, Gating time: 5 ms	25°C	3 V	7.920	8	8.080	MHz
$f_{CAL(12MHz)}$	12-MHz calibration value	BCSCTL1 = CALBC1_12MHZ, DCOCTL = CALDCO_12MHZ, Gating time: 5 ms	25°C	3 V	11.88	12	12.12	MHz
$f_{CAL(16MHz)}$	16-MHz calibration value	BCSCTL1 = CALBC1_16MHZ, DCOCTL = CALDCO_16MHZ, Gating time: 2 ms	25°C	3 V	15.84	16	16.16	MHz

5.21 Calibrated DCO Frequencies – Tolerance Over Temperature 0°C to 85°C

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	V_{CC}	MIN	TYP	MAX	UNIT
	1-MHz tolerance over temperature		0°C to 85°C	3 V	–2.5%	±0.5%	+2.5%	
	8-MHz tolerance over temperature		0°C to 85°C	3 V	–2.5%	±1.0%	+2.5%	
	12-MHz tolerance over temperature		0°C to 85°C	3 V	–2.5%	±1.0%	+2.5%	
	16-MHz tolerance over temperature		0°C to 85°C	3 V	–3%	±2.0%	+3%	
$f_{CAL(1MHz)}$	1-MHz calibration value	BCSCTL1 = CALBC1_1MHZ, DCOCTL = CALDCO_1MHZ, Gating time: 5 ms	0°C to 85°C	2.2 V	0.970	1	1.030	MHz
				3 V	0.975	1	1.025	
				3.6 V	0.970	1	1.030	
$f_{CAL(8MHz)}$	8-MHz calibration value	BCSCTL1 = CALBC1_8MHZ, DCOCTL = CALDCO_8MHZ, Gating time: 5 ms	0°C to 85°C	2.2 V	7.760	8	8.40	MHz
				3 V	7.800	8	8.20	
				3.6 V	7.600	8	8.24	
$f_{CAL(12MHz)}$	12-MHz calibration value	BCSCTL1 = CALBC1_12MHZ, DCOCTL = CALDCO_12MHZ, Gating time: 5 ms	0°C to 85°C	2.2 V	11.64	12	12.36	MHz
				3 V	11.64	12	12.36	
				3.6 V	11.64	12	12.36	
$f_{CAL(16MHz)}$	16-MHz calibration value	BCSCTL1 = CALBC1_16MHZ, DCOCTL = CALDCO_16MHZ, Gating time: 2 ms	0°C to 85°C	3 V	15.52	16	16.48	MHz
				3.6 V	15.00	16	16.48	

5.22 Calibrated DCO Frequencies – Tolerance Over Supply Voltage V_{CC}

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	V_{CC}	MIN	TYP	MAX	UNIT
	1-MHz tolerance over V_{CC}		25°C	1.8 V to 3.6 V	–3%	±2%	+3%	
	8-MHz tolerance over V_{CC}		25°C	1.8 V to 3.6 V	–3%	±2%	+3%	
	12-MHz tolerance over V_{CC}		25°C	2.2 V to 3.6 V	–3%	±2%	+3%	
	16-MHz tolerance over V_{CC}		25°C	3 V to 3.6 V	–6%	±2%	+3%	
$f_{CAL(1MHz)}$	1-MHz calibration value	BCSCTL1 = CALBC1_1MHZ, DCOCTL = CALDCO_1MHZ, Gating time: 5 ms	25°C	1.8 V to 3.6 V	0.97	1	1.03	MHz
$f_{CAL(8MHz)}$	8-MHz calibration value	BCSCTL1 = CALBC1_8MHZ, DCOCTL = CALDCO_8MHZ, Gating time: 5 ms	25°C	1.8 V to 3.6 V	7.76	8	8.24	MHz
$f_{CAL(12MHz)}$	12-MHz calibration value	BCSCTL1 = CALBC1_12MHZ, DCOCTL = CALDCO_12MHZ, Gating time: 5 ms	25°C	2.2 V to 3.6 V	11.64	12	12.36	MHz
$f_{CAL(16MHz)}$	16-MHz calibration value	BCSCTL1 = CALBC1_16MHZ, DCOCTL = CALDCO_16MHZ, Gating time: 2 ms	25°C	3 V to 3.6 V	15	16	16.48	MHz

5.23 Calibrated DCO Frequencies – Overall Tolerance

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	V_{CC}	MIN	TYP	MAX	UNIT
	1-MHz tolerance overall		–40°C to 105°C	1.8 V to 3.6 V	–5%	±2%	+5%	
	8-MHz tolerance overall		–40°C to 105°C	1.8 V to 3.6 V	–5%	±2%	+5%	
	12-MHz tolerance overall		–40°C to 105°C	2.2 V to 3.6 V	–5%	±2%	+5%	
	16-MHz tolerance overall		–40°C to 105°C	3 V to 3.6 V	–6%	±3%	+6%	
$f_{CAL(1MHz)}$	1-MHz calibration value (see Figure 5-14)	BCSCTL1 = CALBC1_1MHZ, DCOCTL = CALDCO_1MHZ, Gating time: 5 ms	–40°C to 105°C	1.8 V to 3.6 V	0.95	1	1.05	MHz
$f_{CAL(8MHz)}$	8-MHz calibration value (see Figure 5-15)	BCSCTL1 = CALBC1_8MHZ, DCOCTL = CALDCO_8MHZ, Gating time: 5 ms	–40°C to 105°C	1.8 V to 3.6 V	7.6	8	8.4	MHz
$f_{CAL(12MHz)}$	12-MHz calibration value (see Figure 5-16)	BCSCTL1 = CALBC1_12MHZ, DCOCTL = CALDCO_12MHZ, Gating time: 5 ms	–40°C to 105°C	2.2 V to 3.6 V	11.4	12	12.6	MHz
$f_{CAL(16MHz)}$	16-MHz calibration value (see Figure 5-17)	BCSCTL1 = CALBC1_16MHZ, DCOCTL = CALDCO_16MHZ, Gating time: 2 ms	–40°C to 105°C	3 V to 3.6 V	15	16	17	MHz

5.24 Typical Characteristics – Calibrated DCO Frequency

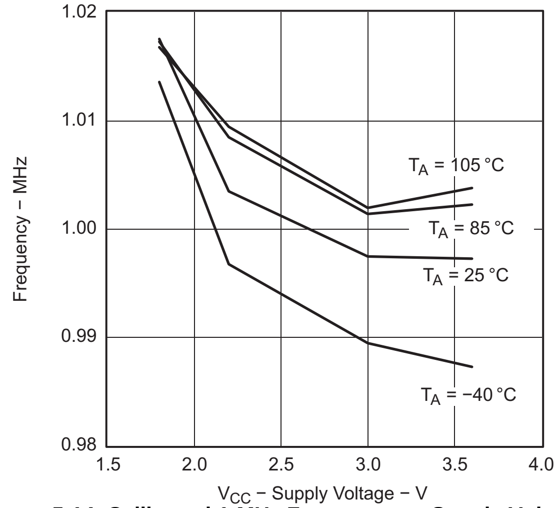


Figure 5-14. Calibrated 1-MHz Frequency vs Supply Voltage

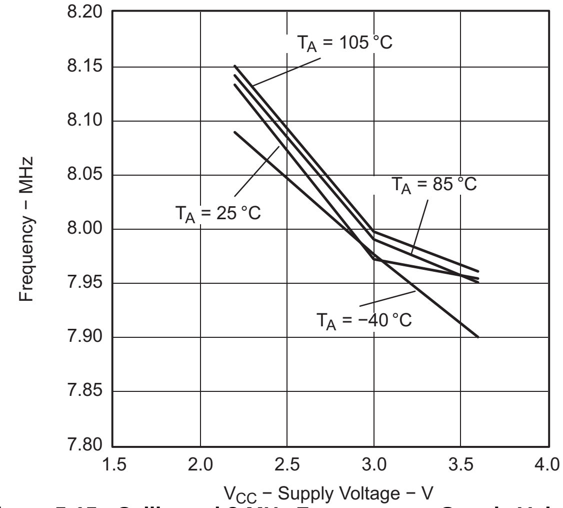


Figure 5-15. Calibrated 8-MHz Frequency vs Supply Voltage

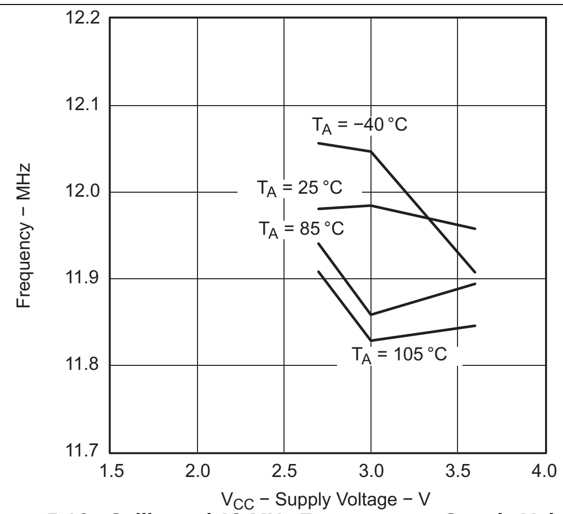


Figure 5-16. Calibrated 12-MHz Frequency vs Supply Voltage

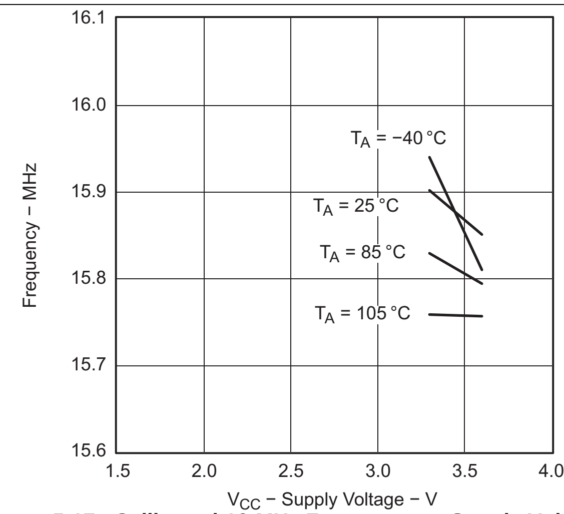


Figure 5-17. Calibrated 16-MHz Frequency vs Supply Voltage

5.25 Wake-up Times From Lower-Power Modes (LPM3, LPM4)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$t_{DCO,LPM3/4}$	DCO clock wake-up time from LPM3 or LPM4 (1) (see Figure 5-18)	BCSCTL1 = CALBC1_1MHZ, DCOCTL = CALDCO_1MHZ	2.2 V, 3 V			2	µs
		BCSCTL1 = CALBC1_8MHZ, DCOCTL = CALDCO_8MHZ				1.5	
		BCSCTL1 = CALBC1_12MHZ, DCOCTL = CALDCO_12MHZ				1	
		BCSCTL1 = CALBC1_16MHZ, DCOCTL = CALDCO_16MHZ	3 V			1	
$t_{CPU,LPM3/4}$	CPU wake-up time from LPM3 or LPM4 (2)					$1 / f_{MCLK} + t_{Clock,LPM3/4}$	

(1) The DCO clock wake-up time is measured from the edge of an external wake-up signal (for example, port interrupt) to the first clock edge observable externally on a clock pin (MCLK or SMCLK).
(2) Parameter applicable only if DCOCLK is used for MCLK.

5.26 Typical Characteristics – DCO Clock Wake-up Time From LPM3 or LPM4

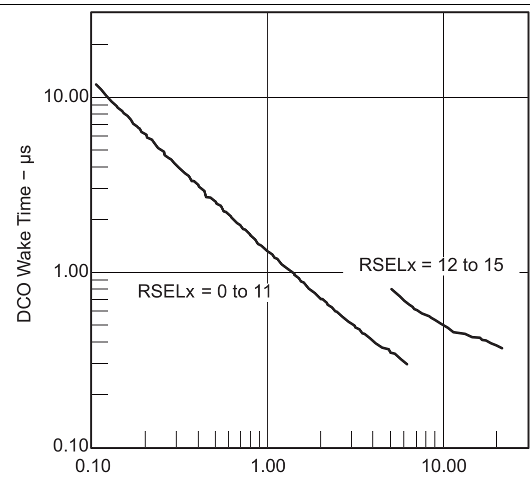


Figure 5-18. DCO Wake-up Time From LPM3 vs DCO Frequency

5.27 DCO With External Resistor R_{OSC}[1]

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)
(see Figure 5-19, Figure 5-20, Figure 5-21, and Figure 5-22)

PARAMETER		TEST CONDITIONS	V_{CC}	TYP	UNIT
$f_{DCO,ROSC}$	DCO output frequency with R_{OSC}	DCOR = 1, RSELx = 4, DCOx = 3, MODx = 0, T_A = 25°C	2.2 V	1.8	MHz
			3 V	1.95	
D_T	Temperature drift	DCOR = 1, RSELx = 4, DCOx = 3, MODx = 0	2.2 V, 3 V	±0.1	%/°C
D_V	Drift with V_{CC}	DCOR = 1, RSELx = 4, DCOx = 3, MODx = 0	2.2 V, 3 V	10	%/V

(1) R_{OSC} = 100 kΩ. Metal film resistor, type 0257, 0.6 W with 1% tolerance and T_K = ±50 ppm/°C.

5.28 Typical Characteristics – DCO With External Resistor R_{OSC}

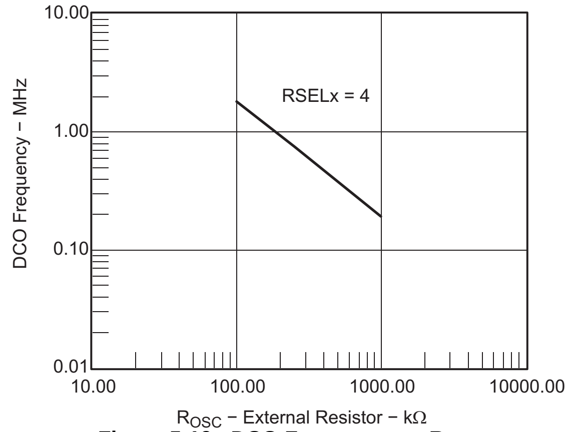


Figure 5-19. DCO Frequency vs R_{OSC} (V_{CC} = 2.2 V, T_A = 25°C)

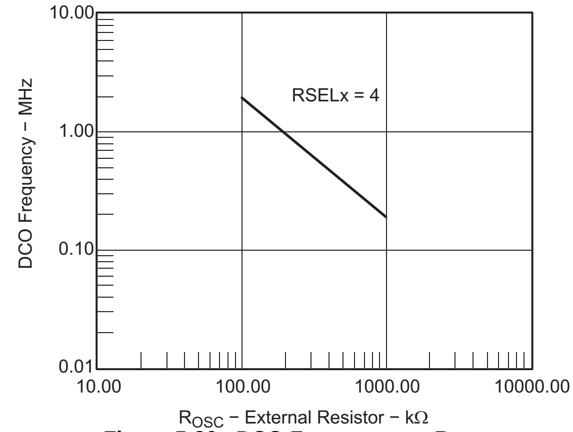


Figure 5-20. DCO Frequency vs R_{OSC} (V_{CC} = 3 V, T_A = 25°C)

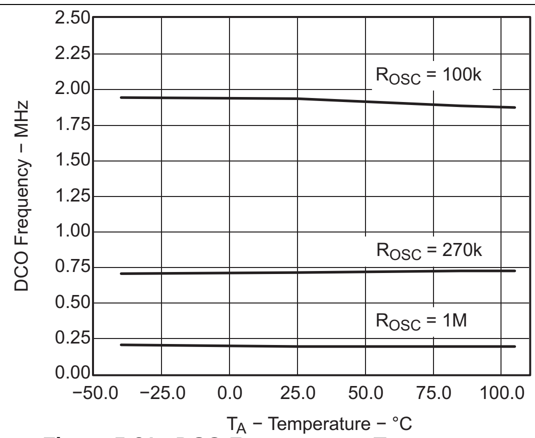


Figure 5-21. DCO Frequency vs Temperature (V_{CC} = 3 V)

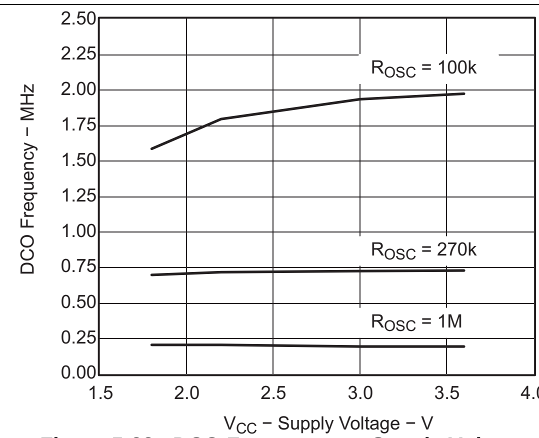


Figure 5-22. DCO Frequency vs Supply Voltage (T_A = 25°C)

5.29 Crystal Oscillator LFXT1, Low-Frequency Mode(1)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$f_{LFXT1,LF}$	LFXT1 oscillator crystal frequency, LF mode 0, 1	XTS = 0, LFXT1Sx = 0 or 1	1.8 V to 3.6 V		32768		Hz
$f_{LFXT1,LF,logic}$	LFXT1 oscillator logic level square wave input frequency, LF mode	XTS = 0, LFXT1Sx = 3, XCAPx = 0	1.8 V to 3.6 V	10000	32768	50000	Hz
OA_{LF}	Oscillation allowance for LF crystals	XTS = 0, LFXT1Sx = 0, $f_{LFXT1,LF}$ = 32768 Hz, $C_{L,eff}$ = 6 pF			500		kΩ
		XTS = 0, LFXT1Sx = 0, $f_{LFXT1,LF}$ = 32768 Hz, $C_{L,eff}$ = 12 pF			200		
$C_{L,eff}$	Integrated effective load capacitance, LF mode(2)	XTS = 0, XCAPx = 0			1		pF
		XTS = 0, XCAPx = 1			5.5		
		XTS = 0, XCAPx = 2			8.5		
		XTS = 0, XCAPx = 3			11		
	Duty cycle, LF mode	XTS = 0, Measured at P2.0/ACLK, $f_{LFXT1,LF}$ = 32768 Hz	2.2 V, 3 V	30%	50%	70%	
$f_{Fault,LF}$	Oscillator fault frequency, LF mode(3)	XTS = 0, LFXT1Sx = 3, XCAPx = 0(4)	2.2 V, 3 V	10		10000	Hz

(1) To improve EMI on the XT1 oscillator, the following guidelines should be observed.
- Keep the trace between the device and the crystal as short as possible.
- Design a good ground plane around the oscillator pins.
- Prevent crosstalk from other clock or data lines into oscillator pins XIN and XOUT.
- Avoid running PCB traces underneath or adjacent to the XIN and XOUT pins.
- Use assembly materials and processes that avoid any parasitic load on the oscillator XIN and XOUT pins.
- If conformal coating is used, make sure that it does not induce capacitive or resistive leakage between the oscillator pins.
- Do not route the XOUT line to the JTAG header to support the serial programming adapter as shown in other documentation. This signal is no longer required for the serial programming adapter.

(2) Includes parasitic bond and package capacitance (approximately 2 pF per pin).
Because the PCB adds additional capacitance, verify the correct load by measuring the ACLK frequency. For a correct setup, the effective load capacitance should always match the specification of the crystal that is used.
(3) Frequencies below the MIN specification set the fault flag. Frequencies above the MAX specification do not set the fault flag. Frequencies in between might set the flag.
(4) Measured with logic-level input frequency but also applies to operation with crystals.

5.30 Internal Very-Low-Power Low-Frequency Oscillator (VLO)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		T_A	V_{CC}	MIN	TYP	MAX	UNIT
f_{VLO}	VLO frequency	–40°C to 85°C	2.2 V, 3 V	4	12	20	kHz
		105°C				22	
df_{VLO}/dT	VLO frequency temperature drift(1)		2.2 V, 3 V		0.5		%/°C
df_{VLO}/dV_{CC}	VLO frequency supply voltage drift(2)	25°C	1.8 V to 3.6 V		4		%/V

(1) Calculated using the box method:
I: (MAX(–40°C to 85°C) – MIN(–40°C to 85°C)) / MIN(–40°C to 85°C) / (85°C – (-40°C))
T: (MAX(–40°C to 105°C) – MIN(–40°C to 105°C)) / MIN(–40°C to 105°C) / (105°C – (-40°C))
(2) Calculated using the box method: (MAX(1.8 V to 3.6 V) – MIN(1.8 V to 3.6 V)) / MIN(1.8 V to 3.6 V) / (3.6 V – 1.8 V)

5.31 Crystal Oscillator LFXT1, High-Frequency Mode[(1)]

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$f_{LFXT1,HF0}$	LFXT1 oscillator crystal frequency, HF mode 0	XTS = 1, LFXT1Sx = 0, XCAPx = 0	1.8 V to 3.6 V	0.4		1	MHz
$f_{LFXT1,HF1}$	LFXT1 oscillator crystal frequency, HF mode 1	XTS = 1, LFXT1Sx = 1, XCAPx = 0	1.8 V to 3.6 V	1		4	MHz
$f_{LFXT1,HF2}$	LFXT1 oscillator crystal frequency, HF mode 2	XTS = 1, LFXT1Sx = 2, XCAPx = 0	1.8 V to 3.6 V	2		10	MHz
			2.2 V to 3.6 V	2		12	
			3 V to 3.6 V	2		16	
$f_{LFXT1,HF,logic}$	LFXT1 oscillator logic-level square-wave input frequency, HF mode	XTS = 1, LFXT1Sx = 3, XCAPx = 0	1.8 V to 3.6 V	0.4		10	MHz
			2.2 V to 3.6 V	0.4		12	
			3 V to 3.6 V	0.4		16	
OA_{HF}	Oscillation allowance for HF crystals (see Figure 5-23 and Figure 5-24)	XTS = 1, XCAPx = 0, LFXT1Sx = 0, $f_{LFXT1,HF}$ = 1 MHz, $C_{L,eff}$ = 15 pF			2700		Ω
		XTS = 1, XCAPx = 0, LFXT1Sx = 1, $f_{LFXT1,HF}$ = 4 MHz, $C_{L,eff}$ = 15 pF			800		
		XTS = 1, XCAPx = 0, LFXT1Sx = 2, $f_{LFXT1,HF}$ = 16 MHz, $C_{L,eff}$ = 15 pF			300		
$C_{L,eff}$	Integrated effective load capacitance, HF mode[(2)]	XTS = 1, XCAPx = 0[(3)]			1		pF
	Duty cycle, HF mode	XTS = 1, XCAPx = 0, Measured at P2.0/ACLK, $f_{LFXT1,HF}$ = 10 MHz	2.2 V, 3 V	40%	50%	60%	
		XTS = 1, XCAPx = 0, Measured at P2.0/ACLK, $f_{LFXT1,HF}$ = 16 MHz	2.2 V, 3 V	40%	50%	60%	
$f_{Fault,HF}$	Oscillator fault frequency[(4)]	XTS = 1, LFXT1Sx = 3, XCAPx = 0[(5)]	2.2 V, 3 V	30		300	kHz

(1) To improve EMI on the XT2 oscillator the following guidelines should be observed:
- Keep the trace between the device and the crystal as short as possible.
- Design a good ground plane around the oscillator pins.
- Prevent crosstalk from other clock or data lines into oscillator pins XIN and XOUT.
- Avoid running PCB traces underneath or adjacent to the XIN and XOUT pins.
- Use assembly materials and processes that avoid any parasitic load on the oscillator XIN and XOUT pins.
- If conformal coating is used, make sure that it does not induce capacitive or resistive leakage between the oscillator pins.
- Do not route the XOUT line to the JTAG header to support the serial programming adapter as shown in other documentation. This signal is no longer required for the serial programming adapter.

(2) Includes parasitic bond and package capacitance (approximately 2 pF per pin). Because the PCB adds additional capacitance, verify the correct load by measuring the ACLK frequency. For a correct setup, the effective load capacitance should always match the specification of the used crystal.
(3) Requires external capacitors at both terminals. Values are specified by crystal manufacturers.
(4) Frequencies below the MIN specification set the fault flag, frequencies above the MAX specification do not set the fault flag, and frequencies in between might set the flag.
(5) Measured with logic-level input frequency, but also applies to operation with crystals.

5.32 Typical Characteristics – LFXT1 Oscillator in HF Mode (XTS = 1)

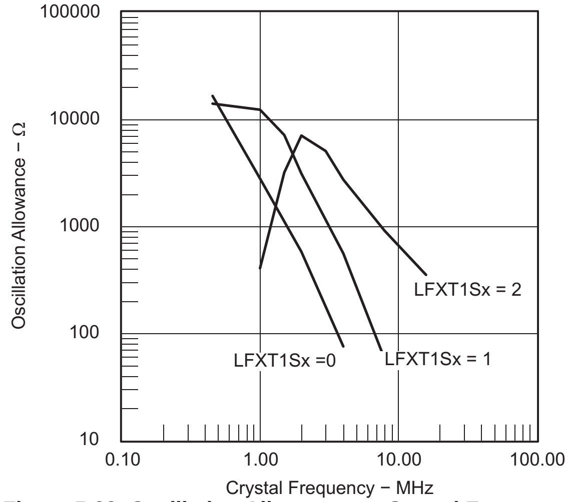


Figure 5-23. Oscillation Allowance vs Crystal Frequency $C_{L,eff}$ = 15 pF, T_A = 25°C

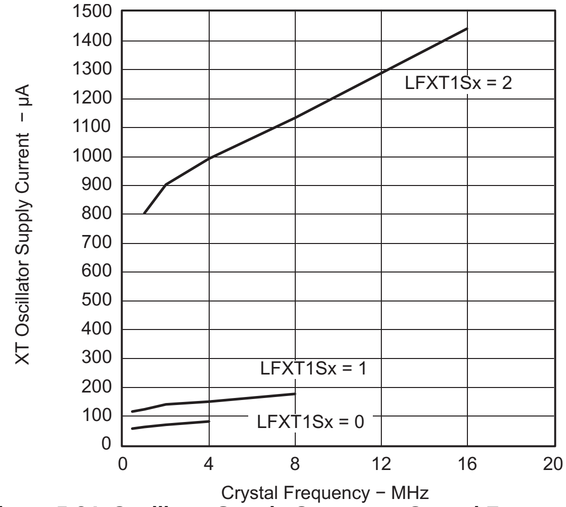


Figure 5-24. Oscillator Supply Current vs Crystal Frequency $C_{L,eff}$ = 15 pF, T_A = 25°C

5.33 Crystal Oscillator XT2[(1)]

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
f_{XT2}	XT2 oscillator crystal frequency, mode 0	XT2Sx = 0	1.8 V to 3.6 V	0.4		1	MHz
f_{XT2}	XT2 oscillator crystal frequency, mode 1	XT2Sx = 1	1.8 V to 3.6 V	1		4	MHz
f_{XT2}	XT2 oscillator crystal frequency, mode 2	XT2Sx = 2	1.8 V to 2.2 V	2		10	MHz
			2.2 V to 3.6 V	2		12	
			3 V to 3.6 V	2		16	
f_{XT2}	XT2 oscillator logic-level square-wave input frequency	XT2Sx = 3	1.8 V to 2.2 V	0.4		10	MHz
			2.2 V to 3.6 V	0.4		12	
			3 V to 3.6 V	0.4		16	
OA	Oscillation allowance (see Figure 5-25 and Figure 5-26)	XT2Sx = 0, f_{XT2} = 1 MHz, $C_{L,eff}$ = 15 pF			2700		Ω
		XT2Sx = 1, f_{XT2} = 4 MHz, $C_{L,eff}$ = 15 pF			800		
		XT2Sx = 2, f_{XT2} = 16 MHz, $C_{L,eff}$ = 15 pF			300		
$C_{L,eff}$	Integrated effective load capacitance, HF mode[(2)]	See [(3)]			1		pF
	Duty cycle	Measured at P1.4/SMCLK, f_{XT2} = 10 MHz	2.2 V, 3 V	40%	50%	60%	
		Measured at P1.4/SMCLK, f_{XT2} = 16 MHz		40%	50%	60%	
f_{Fault}	Oscillator fault frequency, HF mode[(4)]	XT2Sx = 3[(5)]	2.2 V, 3 V	30		300	kHz

(1) To improve EMI on the XT2 oscillator the following guidelines should be observed:
- Keep the trace between the device and the crystal as short as possible.
- Design a good ground plane around the oscillator pins.
- Prevent crosstalk from other clock or data lines into oscillator pins XT2IN and XT2OUT.
- Avoid running PCB traces underneath or adjacent to the XT2IN and XT2OUT pins.
- Use assembly materials and processes that avoid any parasitic load on the oscillator XT2IN and XT2OUT pins.
- If conformal coating is used, make sure that it does not induce capacitive or resistive leakage between the oscillator pins.

(2) Includes parasitic bond and package capacitance (approximately 2 pF per pin). Because the PCB adds additional capacitance, verify the correct load by measuring the ACLK frequency. For a correct setup, the effective load capacitance should always match the specification of the used crystal.

(3) Requires external capacitors at both terminals. Values are specified by crystal manufacturers.

(4) Frequencies below the MIN specification set the fault flag, frequencies above the MAX specification do not set the fault flag, and frequencies in between might set the flag.

(5) Measured with logic-level input frequency, but also applies to operation with crystals.

5.34 Typical Characteristics – XT2 Oscillator

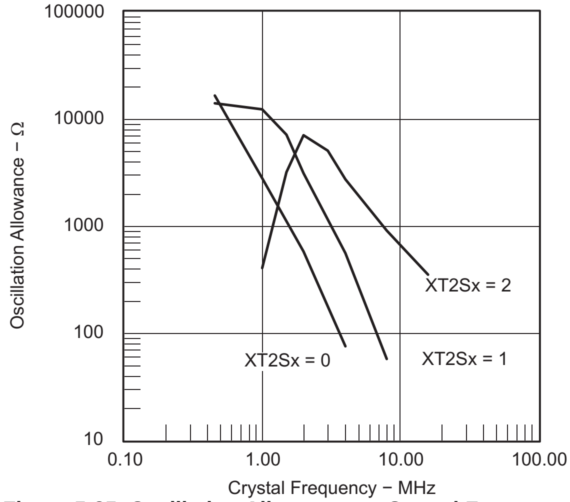


Figure 5-25. Oscillation Allowance vs Crystal Frequency
$C_{L,eff}$ = 15 pF, T_A = 25°C

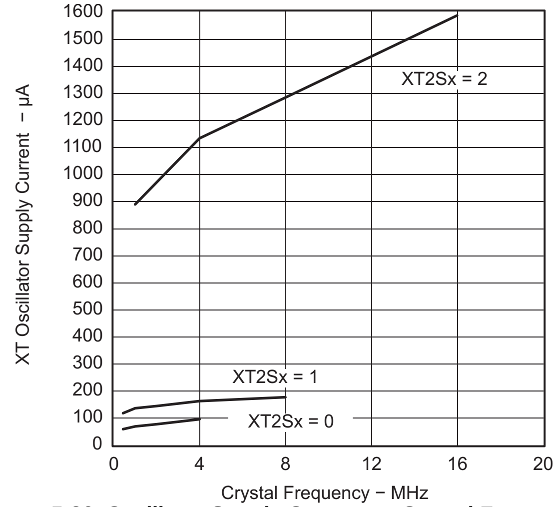


Figure 5-26. Oscillator Supply Current vs Crystal Frequency
$C_{L,eff}$ = 15 pF, T_A = 25°C

5.35 Timer_A

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
f_{TA}	Timer_A clock frequency	Internal: SMCLK or ACLK, External: TACLK or INCLK, Duty cycle = 50% ±10%	2.2 V			10	MHz
			3 V			16	
$t_{TA,cap}$	Timer_A capture timing	TA0, TA1, TA2	2.2 V, 3 V	20			ns

5.36 Timer_B

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
f_{TB}	Timer_B clock frequency	Internal: SMCLK or ACLK, External: TBCLK or INCLK, Duty cycle = 50% ±10%	2.2 V			10	MHz
			3 V			16	
$t_{TB,cap}$	Timer_B capture timing	TB0, TB1, TB2	2.2 V, 3 V	20			ns

5.37 USCI (UART Mode)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
f_{USCI}	USCI input clock frequency	Internal: SMCLK or ACLK, External: UCLK, Duty cycle = 50% ±10%				f_{SYSTEM}	MHz
f_{BITCLK}	BITCLK clock frequency (equals baud rate in MBaud)[1]		2.2 V, 3 V			1	MHz
t_{τ}	UART receive deglitch time[2]		2.2 V	50	150	600	ns
			3 V	50	100	600	

(1) The DCO wake-up time must be considered in LPM3 or LPM4 for baud rates above 1 MHz.
(2) Pulses on the UART receive input (UCxRX) shorter than the UART receive deglitch time are suppressed.

5.38 USCI (SPI Master Mode)[1]

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)
(see Figure 5-27 and Figure 5-28)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	MAX	UNIT
f_{USCI}	USCI input clock frequency	SMCLK, ACLK Duty cycle = 50% ±10%			f_{SYSTEM}	MHz
$t_{SU,MI}$	SOMI input data setup time		2.2 V	110		ns
			3 V	75		
$t_{HD,MI}$	SOMI input data hold time		2.2 V	0		ns
			3 V	0		
$t_{VALID,MO}$	SIMO output data valid time	UCLK edge to SIMO valid, C_L = 20 pF	2.2 V		30	ns
			3 V		20	

(1) $f_{UCxCLK} = 1/2t_{LO/HI}$ with $t_{LO/HI} \geq \max(t_{VALID,MO(USCI)} + t_{SU,SI(Slave)}, t_{SU,MI(USCI)} + t_{VALID,SO(Slave)})$
For the slave parameters $t_{SU,SI(Slave)}$ and $t_{VALID,SO(Slave)}$, see the SPI parameters of the attached slave.

5.39 USCI (SPI Slave Mode)(1)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 5-29 and Figure 5-30)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$t_{STE,LEAD}$	STE lead time, STE low to clock		2.2 V, 3 V		50		ns
$t_{STE,LAG}$	STE lag time, last clock to STE high		2.2 V, 3 V	10			ns
$t_{STE,ACC}$	STE access time, STE low to SOMI data out		2.2 V, 3 V		50		ns
$t_{STE,DIS}$	STE disable time, STE high to SOMI high impedance		2.2 V, 3 V		50		ns
$t_{SU,SI}$	SIMO input data setup time		2.2 V	20			ns
			3 V	15			
$t_{HD,SI}$	SIMO input data hold time		2.2 V	10			ns
			3 V	10			
$t_{VALID,SO}$	SOMI output data valid time	UCLK edge to SOMI valid, C_L = 20 pF	2.2 V		75	110	ns
			3 V		50	75	

(1) $f_{UCxCLK} = 1/2t_{LO/HI}$ with $t_{LO/HI} \geq \max(t_{VALID,MO(Master)} + t_{SU,SI(USCI)}, t_{SU,MI(Master)} + t_{VALID,SO(USCI)})$
For the master parameters $t_{SU,MI(Master)}$ and $t_{VALID,MO(Master)}$, see the SPI parameters of the attached master.

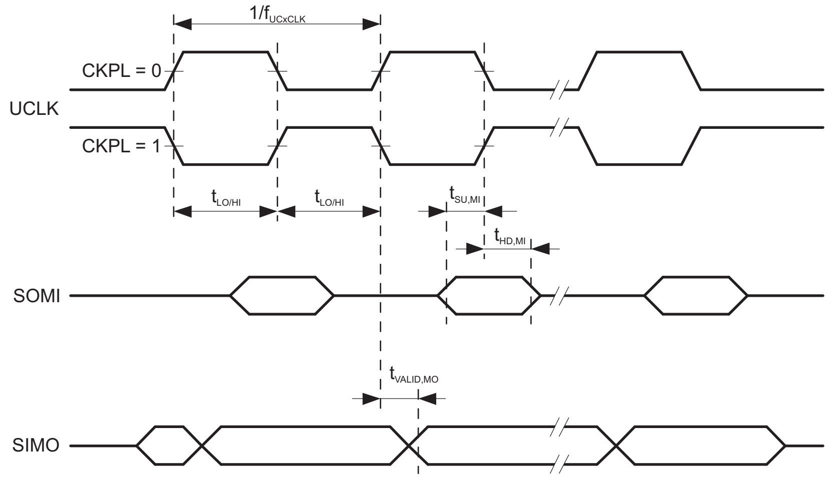


Figure 5-27. SPI Master Mode, CKPH = 0

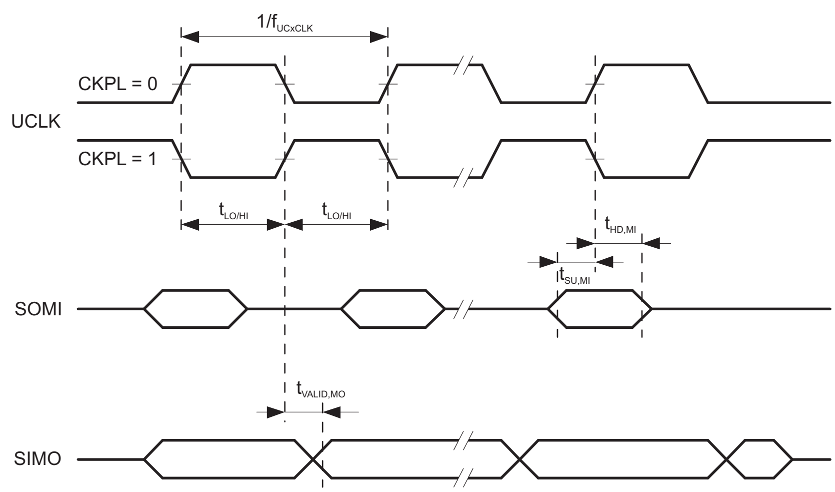


Figure 5-28. SPI Master Mode, CKPH = 1

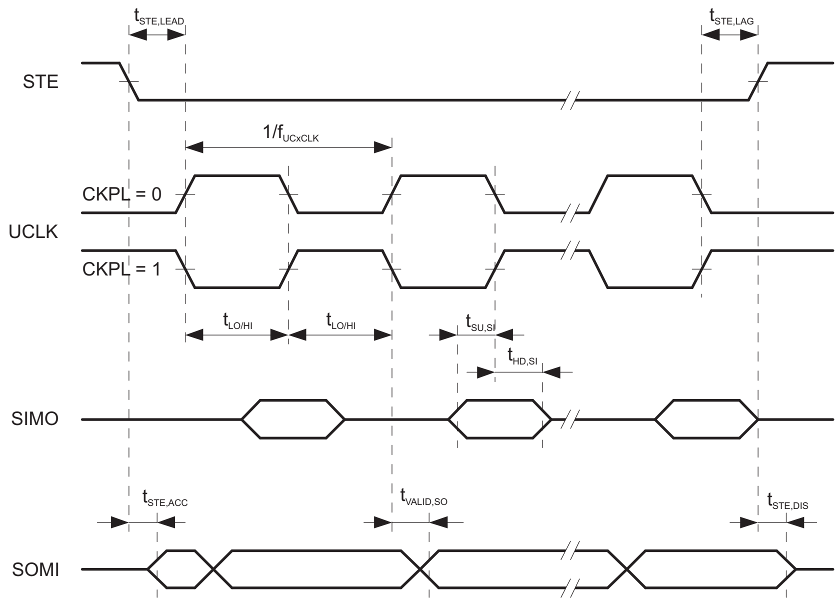


Figure 5-29. SPI Slave Mode, CKPH = 0

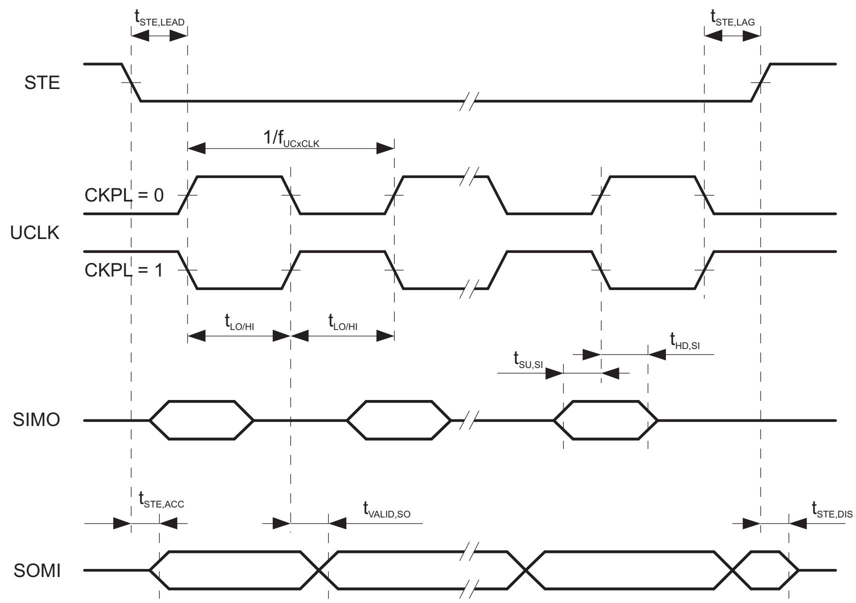


Figure 5-30. SPI Slave Mode, CKPH = 1

5.40 USCI (I^2C Mode)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 5-31)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
f_{USCI}	USCI input clock frequency	Internal: SMCLK or ACLK, External: UCLK, Duty cycle = 50% ±10%				f_{SYSTEM}	MHz
f_{SCL}	SCL clock frequency		2.2 V, 3 V	0		400	kHz
$t_{HD,STA}$	Hold time (repeated) START	f_{SCL} ≤ 100 kHz	2.2 V, 3 V	4			µs
		f_{SCL} > 100 kHz		0.6			
$t_{SU,STA}$	Setup time for a repeated START	f_{SCL} ≤ 100 kHz	2.2 V, 3 V	4.7			µs
		f_{SCL} > 100 kHz		0.6			
$t_{HD,DAT}$	Data hold time		2.2 V, 3 V	0			ns
$t_{SU,DAT}$	Data setup time		2.2 V, 3 V	250			ns
$t_{SU,STO}$	Setup time for STOP		2.2 V, 3 V	4			µs
t_{SP}	Pulse duration of spikes suppressed by input filter		2.2 V	50	150	600	ns
			3 V	50	100	600	

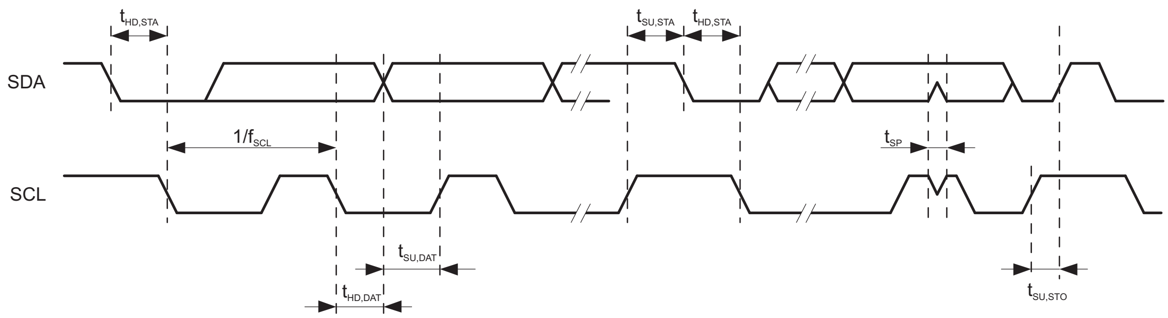


Figure 5-31. I^2C Mode Timing

5.41 Comparator_A+(1)(2)

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$I_{(DD)}$		CAON = 1, CARSEL = 0, CAREF = 0	2.2 V		25	40	µA
			3 V		45	60	
$I_{(Refladder/RefDiode)}$		CAON = 1, CARSEL = 0, CAREF = 1/2/3, No load at P2.3/CA0/TA1 and P2.4/CA1/TA2	2.2 V		30	50	µA
			3 V		45	71	
V_{IC}	Common-mode input voltage range	CAON = 1	2.2 V, 3 V	0		V_{CC} – 1	V
$V_{(Ref025)}$	(Voltage at 0.25 V_{CC} node) ÷ V_{CC}	PCA0 = 1, CARSEL = 1, CAREF = 1, No load at P2.3/CA0/TA1 and P2.4/CA1/TA2	2.2 V, 3 V	0.23	0.24	0.25	
$V_{(Ref050)}$	(Voltage at 0.5 V_{CC} node) ÷ V_{CC}	PCA0 = 1, CARSEL = 1, CAREF = 2, No load at P2.3/CA0/TA1 and P2.4/CA1/TA2	2.2 V, 3 V	0.47	0.48	0.5	
$V_{(RefVT)}$	See Figure 5-35 and Figure 5-36	PCA0 = 1, CARSEL = 1, CAREF = 3, No load at P2.3/CA0/TA1 and P2.4/CA1/TA2, T_A = 85°C	2.2 V	390	480	540	mV
			3 V	400	490	550	
$V_{(offset)}$	Offset voltage(3)		2.2 V, 3 V	–30		30	mV
V_{hys}	Input hysteresis	CAON = 1	2.2 V, 3 V	0	0.7	1.4	mV
$t_{(response)}$	Response time, low to high and high to low(4) (see Figure 5-32 and Figure 5-33)	T_A = 25°C, Overdrive 10 mV, Without filter: CAF = 0	2.2 V	80	165	300	ns
			3 V	70	120	240	
		T_A = 25°C, Overdrive 10 mV, With filter: CAF = 1	2.2 V	1.4	1.9	2.8	µs
			3 V	0.9	1.5	2.2	

(1) The leakage current for the Comparator_A+ terminals is identical to $I_{lkg(Px.y)}$ specification.
(2) Also see Figure 5-34 and Figure 5-37.
(3) The input offset voltage can be cancelled by using the CAEX bit to invert the Comparator_A+ inputs on successive measurements. The two successive measurements are then summed together.
(4) The response time is measured at P2.2/CAOUT/TA0/CA4 with an input voltage step and with Comparator_A+ already enabled (CAON = 1). If CAON is set at the same time, a settling time of up to 300 ns is added to the response time.

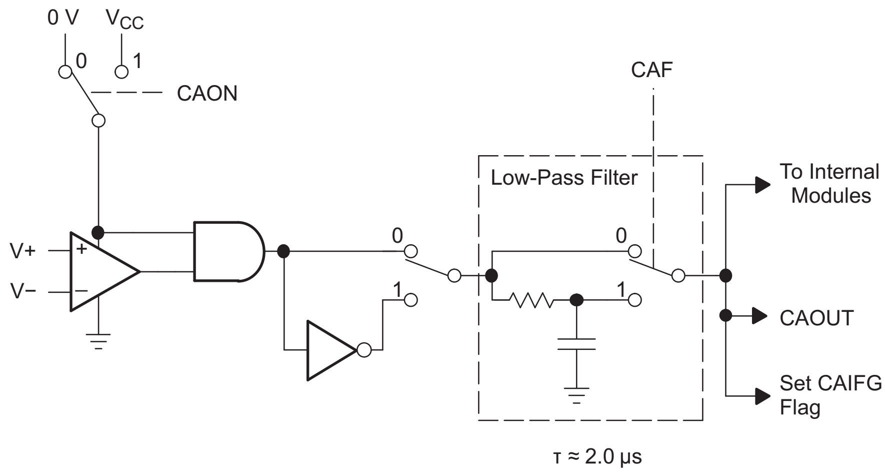


Figure 5-32. Comparator_A+ Module Block Diagram

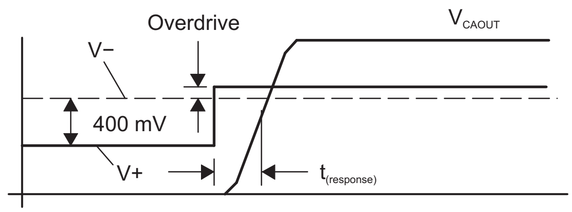


Figure 5-33. Overdrive Definition

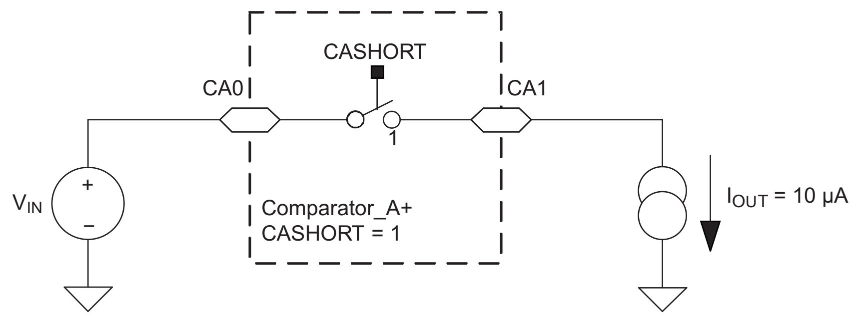


Figure 5-34. Comparator_A+ Short Resistance Test Condition

5.42 Typical Characteristics, Comparator_A+

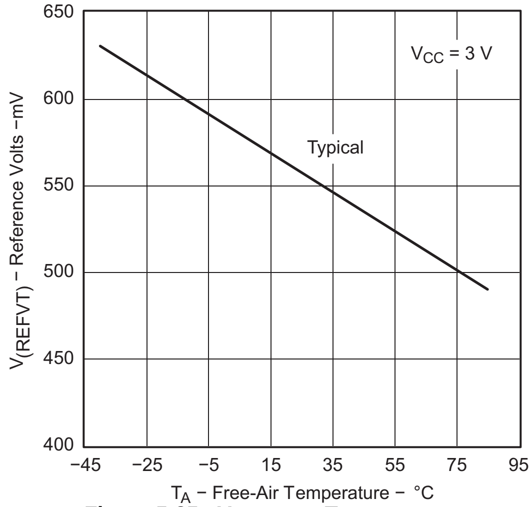


Figure 5-35. $V_{(RefVT)}$ vs Temperature (V_{CC} = 3 V)

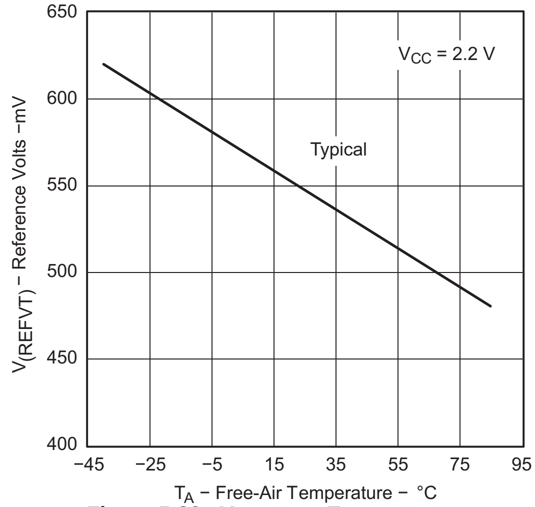


Figure 5-36. $V_{(RefVT)}$ vs Temperature (V_{CC} = 2.2 V)

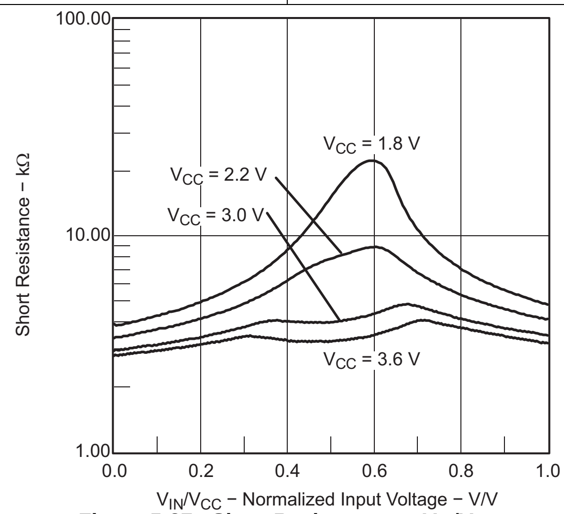


Figure 5-37. Short Resistance vs V_{IN}/V_{CC}

5.43 12-Bit ADC Power Supply and Input Range Conditions [(1)]

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
AV_{CC}	Analog supply voltage	AV_{CC} and DV_{CC} are connected together, AV_{SS} and DV_{SS} are connected together, $V_{(AVSS)} = V_{(DVSS)} = 0$ V		2.2		3.6	V
$V_{(P6.x/Ax)}$	Analog input voltage range[(2)]	All P6.0/A0 to P6.7/A7 terminals, Analog inputs selected in ADC12MCTLx register, P6Sel.x = 1, $0 \le x \le 7$, $V_{(AVSS)} \le V_{P6.x/Ax} \le V_{(AVCC)}$		0		V_{AVCC}	V
I_{ADC12}	Operating supply current into AV_{CC} terminal[(3)]	$f_{ADC12CLK} = 5$ MHz, ADC12ON = 1, REFON = 0, SHT0 = 0, SHT1 = 0, ADC12DIV = 0	2.2 V		0.65	0.8	mA
			3 V		0.8	1	
I_{REF+}	Operating supply current into AV_{CC} terminal[(4)]	$f_{ADC12CLK} = 5$ MHz, ADC12ON = 0, REFON = 1, REF2_5V = 1	3 V		0.5	0.7	mA
		$f_{ADC12CLK} = 5$ MHz, ADC12ON = 0, REFON = 1, REF2_5V = 0	2.2 V		0.5	0.7	
			3 V		0.5	0.7	
C_I	Input capacitance[(5)]	Only one terminal can be selected at one time, P6.x/Ax	2.2 V			40	pF
R_I	Input MUX ON resistance[(5)]	$0 \text{ V} \le V_{Ax} \le V_{AVCC}$	3 V			2000	Ω

(1) The leakage current is defined in the leakage current table with P6.x/Ax parameter.
(2) The analog input voltage range must be within the selected reference voltage range V_{R+} to V_{R-} for valid conversion results.
(3) The internal reference supply current is not included in current consumption parameter I_{ADC12}.
(4) The internal reference current is supplied via terminal AV_{CC}. Consumption is independent of the ADC12ON control bit, unless a conversion is active. The REFON bit enables settling of the built-in reference before starting an A/D conversion.
(5) Not production tested, limits verified by design.

5.44 12-Bit ADC External Reference[(1)]

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	MAX	UNIT
V_{eREF+}	Positive external reference voltage input	$V_{eREF+} > V_{REF-}/V_{eREF-}$ [(2)]		1.4	V_{AVCC}	V
V_{REF-}/V_{eREF-}	Negative external reference voltage input	$V_{eREF+} > V_{REF-}/V_{eREF-}$ [(3)]		0	1.2	V
$(V_{eREF+} - V_{REF-}/V_{eREF-})$	Differential external reference voltage input	$V_{eREF+} > V_{REF-}/V_{eREF-}$ [(4)]		1.4	V_{AVCC}	V
I_{VeREF+}	Static leakage current	$0 \text{ V} \le V_{eREF+} \le V_{AVCC}$	2.2 V, 3 V		±1	µA
$I_{VREF-/VeREF-}$	Static leakage current	$0 \text{ V} \le V_{eREF-} \le V_{AVCC}$	2.2 V, 3 V		±1	µA

(1) The external reference is used during conversion to charge and discharge the capacitance array. The input capacitance, C_I, is also the dynamic load for an external reference during conversion. The dynamic impedance of the reference supply should follow the recommendations on analog-source impedance to allow the charge to settle for 12-bit accuracy.
(2) The accuracy limits the minimum positive external reference voltage. Lower reference voltage levels may be applied with reduced accuracy requirements.
(3) The accuracy limits the maximum negative external reference voltage. Higher reference voltage levels may be applied with reduced accuracy requirements.
(4) The accuracy limits minimum external differential reference voltage. Lower differential reference voltage levels may be applied with reduced accuracy requirements.

5.45 12-Bit ADC Built-In Reference

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 5-39 and Figure 5-40)

PARAMETER		TEST CONDITIONS	T_A	V_{CC}	MIN	TYP	MAX	UNIT
V_{REF+}	Positive built-in reference voltage output	REF2_5V = 1 for 2.5 V, $I_{VREF+}max \le I_{VREF+} \le I_{VREF+}min$	–40°C to 85°C	3 V	2.4	2.5	2.6	V
			105°C		2.37	2.5	2.64	
		REF2_5V = 0 for 1.5 V, $I_{VREF+}max \le I_{VREF+} \le I_{VREF+}min$	–40°C to 85°C	2.2 V, 3 V	1.44	1.5	1.56	
			105°C		1.42	1.5	1.57	
$AV_{CC(min)}$	AV_{CC} minimum voltage, positive built-in reference active	REF2_5V = 0, $I_{VREF+}max \le I_{VREF+} \le I_{VREF+}min$			2.2			V
		REF2_5V = 1, $–0.5\ mA \le I_{VREF+} \le I_{VREF+}min$			2.8			
		REF2_5V = 1, $–1\ mA \le I_{VREF+} \le I_{VREF+}min$			2.9			
I_{VREF+}	Load current out of V_{REF+} terminal			2.2 V	0.01		–0.5	mA
				3 V	0.01		–1	
$I_{L(VREF)+}$	Load-current regulation, V_{REF+} terminal (1)	I_{VREF+} = 500 µA ±100 µA, Analog input voltage ≈ 0.75 V, REF2_5V = 0		2.2 V			±2	LSB
				3 V			±2	
		I_{VREF+} = 500 µA ±100 µA, Analog input voltage ≈ 1.25 V, REF2_5V = 1		3 V			±2	
$I_{DL(VREF)+}$	Load current regulation, V_{REF+} terminal (2)	I_{VREF+} = 100 µA → 900 µA, C_{VREF+} = 5 µF, Ax ≈ 0.5 × V_{REF+}, Error of conversion result ≤ 1 LSB		3 V			20	ns
C_{VREF+}	Capacitance at pin V_{REF+} (3)	REFON = 1, $0\ mA \le I_{VREF+} \le I_{VREF+}max$		2.2 V, 3 V	5	10		µF
T_{REF+}	Temperature coefficient of built-in reference (2)	I_{VREF+} is a constant in the range of $0\ mA \le I_{VREF+} \le 1\ mA$		2.2 V, 3 V			±100	ppm/°C
t_{REFON}	Settling time of internal reference voltage (see Figure 5-38) (2) (4)	I_{VREF+} = 0.5 mA, C_{VREF+} = 10 µF, V_{REF+} = 1.5 V, V_{AVCC} = 2.2 V		2.2 V			17	ms

(1) Not production tested, limits characterized
(2) Not production tested, limits verified by design
(3) The internal buffer operational amplifier and the accuracy specifications require an external capacitor. All INL and DNL tests use two capacitors between pins V_{REF+} and AV_{SS} and between V_{REF-}/V_{eREF-} and AV_{SS}: 10-µF tantalum and 100-nF ceramic.
(4) The condition is that the error in a conversion started after t_{REFON} is less than ±0.5 LSB. The settling time depends on the external capacitive load.

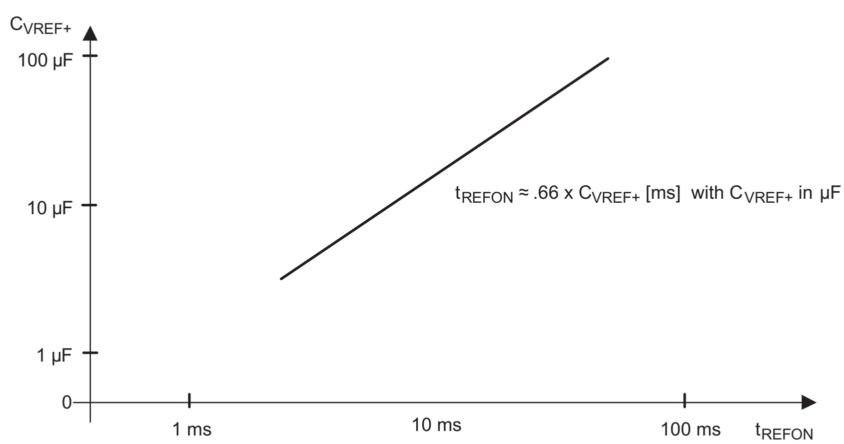


Figure 5-38. Typical Settling Time of Internal Reference t_{REFON} vs External Capacitor on V_{REF+}

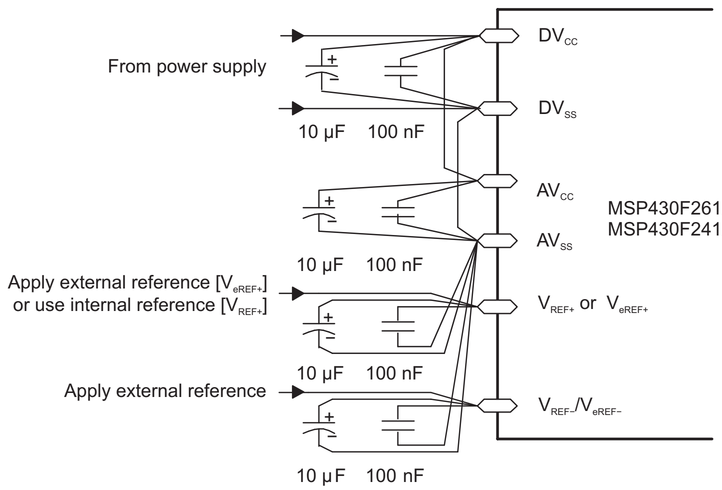


Figure 5-39. Supply Voltage and Reference Voltage Design V_{REF-}/V_{eREF-} External Supply

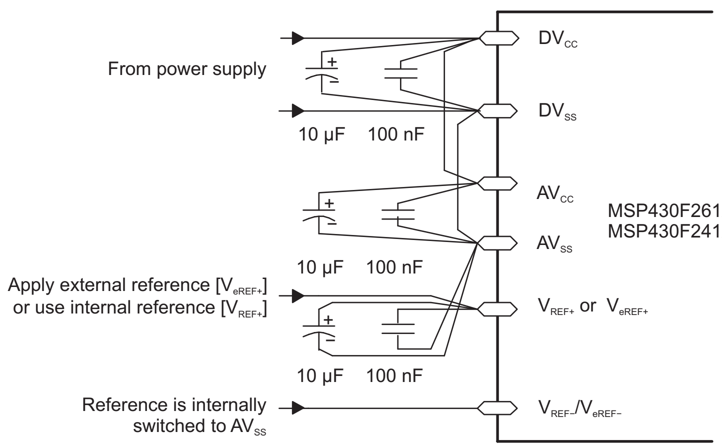


Figure 5-40. Supply Voltage and Reference Voltage Design $V_{REF-}/V_{eREF-} = AV_{SS}$, Internally Connected

5.46 12-Bit ADC Timing Parameters

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$f_{ADC12CLK}$		For specified performance of ADC12 linearity parameters	2.2 V, 3 V	0.45	5	6.3	MHz
$f_{ADC12OSC}$	Internal ADC12 oscillator	ADC12DIV = 0, $f_{ADC12CLK} = f_{ADC12OSC}$	2.2 V, 3 V	3.7	5	6.3	MHz
$t_{CONVERT}$	Conversion time	$C_{VREF+} \geq 5$ µF, Internal oscillator, $f_{ADC12OSC}$ = 3.7 MHz to 6.3 MHz	2.2 V, 3 V	2.06		3.51	µs
		External $f_{ADC12CLK}$ from ACLK, MCLK, or SMCLK, ADC12SSEL ≠ 0			13 × ADC12DIV × $1/f_{ADC12CLK}$		
$t_{ADC12ON}$	Turn-on settling time of the ADC (1)	See (2)				100	ns
t_{Sample}	Sampling time (1)	$R_S = 400\ \Omega, R_I = 1000\ \Omega, C_I = 30$ pF, $\tau = [R_S + R_I] \times C_I$ (3)	3 V	1220			ns
			2.2 V	1400			

(1) Limits verified by design
(2) The condition is that the error in a conversion started after $t_{ADC12ON}$ is less than ±0.5 LSB. The reference and input signal are already settled.
(3) Approximately 10 Tau (τ) are needed to get an error of less than ±0.5 LSB:
$t_{Sample} = \ln(2^{n+1}) \times (R_S + R_I) \times C_I + 800$ ns, where n = ADC resolution = 12, R_S = external source resistance

5.47 12-Bit ADC Linearity Parameters

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
E_I	Integral linearity error	$1.4\ V \leq (V_{eREF+} - V_{REF-}/V_{eREF-})$ min ≤ 1.6 V	2.2 V, 3 V			±2	LSB
		$1.6\ V < (V_{eREF+} - V_{REF-}/V_{eREF-})$ min $\leq V_{AVCC}$				±1.7	
E_D	Differential linearity error	$(V_{eREF+} - V_{REF-}/V_{eREF-})$ min $\leq (V_{eREF+} - V_{REF-}/V_{eREF-})$, C_{VREF+} = 10 µF (tantalum) and 100 nF (ceramic)	2.2 V, 3 V			±1	LSB
E_O	Offset error	$(V_{eREF+} - V_{REF-}/V_{eREF-})$ min $\leq (V_{eREF+} - V_{REF-}/V_{eREF-})$, Internal impedance of source RS < 100 Ω, C_{VREF+} = 10 µF (tantalum) and 100 nF (ceramic)	2.2 V, 3 V		±2	±4	LSB
E_G	Gain error	$(V_{eREF+} - V_{REF-}/V_{eREF-})$ min $\leq (V_{eREF+} - V_{REF-}/V_{eREF-})$, C_{VREF+} = 10 µF (tantalum) and 100 nF (ceramic)	2.2 V, 3 V		±1.1	±2	LSB
E_T	Total unadjusted error	$(V_{eREF+} - V_{REF-}/V_{eREF-})$ min $\leq (V_{eREF+} - V_{REF-}/V_{eREF-})$, C_{VREF+} = 10 µF (tantalum) and 100 nF (ceramic)	2.2 V, 3 V		±2	±5	LSB

5.48 12-Bit ADC Temperature Sensor and Built-In V_{MID}

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
I_{SENSOR}	Operating supply current into AV_{CC} terminal (1)	REFON = 0, INCH = 0Ah, ADC12ON = 1, T_A = 25°C	2.2 V		40	120	µA
			3 V		60	160	
V_{SENSOR}	Temperature sensor voltage (2) (3)	ADC12ON = 1, INCH = 0Ah, T_A = 0°C	2.2 V		986		mV
			3 V		986		
TC_{SENSOR}	Temperature coefficient (3)	ADC12ON = 1, INCH = 0Ah	2.2 V		3.55		mV/°C
			3 V		3.55		
$t_{SENSOR(sample)}$	Sample time required if channel 10 is selected (4) (3)	ADC12ON = 1, INCH = 0Ah, Error of conversion result ≤ 1 LSB	2.2 V	30			µs
			3 V	30			
I_{VMID}	Current into divider at channel 11 (5)	ADC12ON = 1, INCH = 0Bh	2.2 V			N/A (5)	µA
			3 V			N/A (5)	
V_{MID}	AV_{CC} divider at channel 11	ADC12ON = 1, INCH = 0Bh, $V_{MID} \approx 0.5 \times V_{AVCC}$	2.2 V		1.1	1.1 ±0.04	V
			3 V		1.5	1.5 ±0.04	
$t_{VMID(sample)}$	Sample time required if channel 11 is selected (6)	ADC12ON = 1, INCH = 0Bh, Error of conversion result ≤ 1 LSB	2.2 V	1400			ns
			3 V	1220			

(1) The sensor current I_{SENSOR} is consumed if (ADC12ON = 1 and REFON = 1), or (ADC12ON = 1 AND INCH = 0Ah and sample signal is high). Therefore it includes the constant current through the sensor and the reference.
(2) The temperature sensor offset can be as much as ±20°C. TI recommends a single-point calibration to minimize the offset error of the built-in temperature sensor.
(3) Limits characterized
(4) The typical equivalent impedance of the sensor is 51 kΩ. The sample time required includes the sensor-on time $t_{SENSOR(on)}$
(5) No additional current is needed. The V_{MID} is used during sampling.
(6) The on-time $t_{VMID(on)}$ is included in the sampling time $t_{VMID(sample)}$, no additional on time is needed.

5.49 12-Bit DAC Supply Specifications

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	T_A	MIN	TYP	MAX	UNIT
AV_{CC}	Analog supply voltage	$AV_{CC} = DV_{CC}$, $AV_{SS} = DV_{SS}$ = 0 V			2.2		3.6	V
I_{DD}	Supply current, single DAC channel (1) (2)	DAC12AMPx = 2, DAC12IR = 0, DAC12_xDAT = 0x0800	2.2 V, 3 V	–40°C to 85°C		50	110	µA
				105°C		69	150	
		DAC12AMPx = 2, DAC12IR = 1, DAC12_xDAT = 0x0800, $V_{eREF+} = V_{REF+} = AV_{CC}$	2.2 V, 3 V			50	130	
		DAC12AMPx = 5, DAC12IR = 1, DAC12_xDAT = 0x0800, $V_{eREF+} = V_{REF+} = AV_{CC}$	2.2 V, 3 V			200	440	
		DAC12AMPx = 7, DAC12IR = 1, DAC12_xDAT = 0x0800, $V_{eREF+} = V_{REF+} = AV_{CC}$	2.2 V, 3 V			700	1500	
PSRR	Power-supply rejection ratio (3) (4)	DAC12_xDAT = 800h, V_{REF} = 1.5 V, ΔAV_{CC} = 100 mV	2.2 V			70		dB
		DAC12_xDAT = 800h, V_{REF} = 1.5 V or 2.5 V, ΔAV_{CC} = 100 mV	3 V			70		

(1) No load at the output pin, DAC12_0 or DAC12_1, assuming that the control bits for the shared pins are set properly.
(2) Current into reference terminals not included. If DAC12IR = 1 current flows through the input divider; see Reference Input specifications.
(3) PSRR = 20 × log($\Delta AV_{CC}/\Delta V_{DAC12\_xOUT}$)
(4) V_{REF} is applied externally. The internal reference is not used.

5.50 12-Bit DAC Linearity Specifications

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 5-41)

PARAMETER	TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
Resolution	12-bit monotonic		12			bits

12-Bit DAC Linearity Specifications *(continued)*

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 5-41)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
INL	Integral nonlinearity(1) (see Figure 5-42)	V_{REF} = 1.5 V, DAC12AMPx = 7, DAC12IR = 1	2.2 V		±2.0	±8.0	LSB
		V_{REF} = 2.5 V, DAC12AMPx = 7, DAC12IR = 1	3 V		±2.0	±8.0	
DNL	Differential nonlinearity(1) (see Figure 5-43)	V_{REF} = 1.5 V, DAC12AMPx = 7, DAC12IR = 1	2.2 V		±0.4	±1.0	LSB
		V_{REF} = 2.5 V, DAC12AMPx = 7, DAC12IR = 1	3 V		±0.4	±1.0	
E_O	Offset voltage without calibration(1)(2)	V_{REF} = 1.5 V, DAC12AMPx = 7, DAC12IR = 1	2.2 V			±21	mV
		V_{REF} = 2.5 V, DAC12AMPx = 7, DAC12IR = 1	3 V			±21	
	Offset voltage with calibration(1)(2)	V_{REF} = 1.5 V, DAC12AMPx = 7, DAC12IR = 1	2.2 V			±2.5	
		V_{REF} = 2.5 V, DAC12AMPx = 7, DAC12IR = 1	3 V			±2.5	
$d_{E(O)}/d_T$	Offset error temperature coefficient(1)		2.2 V, 3 V		30		µV/C
E_G	Gain error(1)	V_{REF} = 1.5 V	2.2 V			±3.50	% FSR
		V_{REF} = 2.5 V	3 V			±3.50	
$d_{E(G)}/d_T$	Gain temperature coefficient(1)		2.2 V, 3 V		10		ppm of FSR/°C
t_{Offset_Cal}	Time for offset calibration(3)	DAC12AMPx = 2	2.2 V, 3 V			100	ms
		DAC12AMPx = 3, 5				32	
		DAC12AMPx = 4, 6, 7				6	

(1) Parameters calculated from the best-fit curve from 0x0A to 0xFFF. The best-fit curve method is used to deliver coefficients "a" and "b" of the first-order equation: y = a + b × x. $VDAC12\_xOUT = E_O + (1 + E_G) \times (V_{eREF+} / 4095) \times DAC12\_xDAT$, DAC12IR = 1.
(2) The offset calibration works on the output operational amplifier. Offset calibration is triggered setting bit DAC12CALON.
(3) The offset calibration can be done if DAC12AMPx = {2, 3, 4, 5, 6, 7}. The output operational amplifier is switched off with DAC12AMPx= {0, 1}. The DAC12 module should be configured before initiating calibration. Port activity during calibration may affect accuracy and is not recommended.

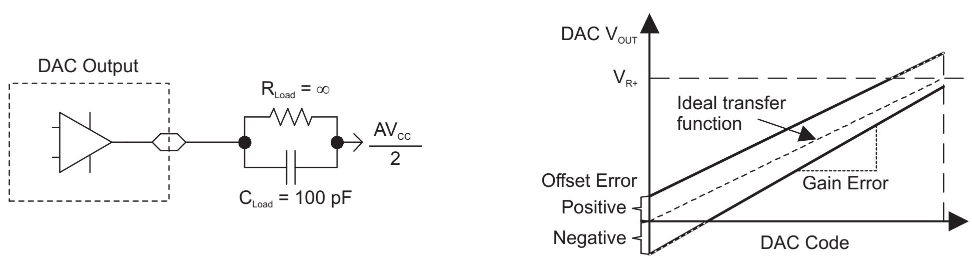


Figure 5-41. Linearity Test Load Conditions, Gain and Offset Definition

5.51 Typical Characteristics, 12-Bit DAC Linearity Specifications

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

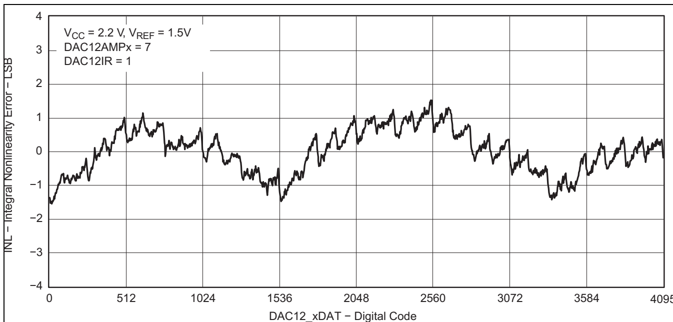


Figure 5-42. Typical INL Error vs Digital Input Data

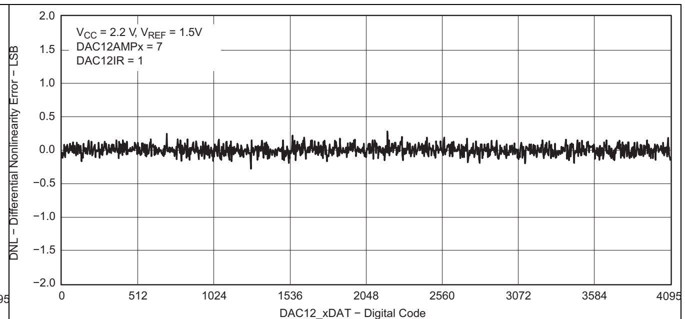


Figure 5-43. Typical DNL Error vs Digital Input Data

5.52 12-Bit DAC Output Specifications

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
V_O	Output voltage range(1) (see Figure 5-44)	No Load, $V_{eREF+} = AV_{CC}$, DAC12_xDAT = 0h, DAC12IR = 1, DAC12AMPx = 7	2.2 V, 3 V	0		0.005	V
		No Load, $V_{eREF+} = AV_{CC}$, DAC12_xDAT = 0FFFh, DAC12IR = 1, DAC12AMPx = 7		AV_{CC} – 0.05		AV_{CC}	
		R_{Load} = 3 kΩ, $V_{eREF+} = AV_{CC}$, DAC12_xDAT = 0h, DAC12IR = 1, DAC12AMPx = 7		0		0.1	
		R_{Load} = 3 kΩ, $V_{eREF+} = AV_{CC}$, DAC12_xDAT = 0FFFh, DAC12IR = 1, DAC12AMPx = 7		AV_{CC} – 0.13		AV_{CC}	
$C_{L(DAC12)}$	Maximum DAC12 load capacitance		2.2 V, 3 V			100	pF
$I_{L(DAC12)}$	Maximum DAC12 load current		2.2 V	–0.5		0.5	mA
			3 V	–1		1	
$R_{O/P(DAC12)}$	Output resistance (see Figure 5-44)	R_{Load} = 3 kΩ, $V_{O/P(DAC12)}$ = 0 V, DAC12AMPx = 7, DAC12_xDAT = 0h	2.2 V, 3 V		150	250	Ω
		R_{Load} = 3 kΩ, $V_{O/P(DAC12)} = AV_{CC}$, DAC12AMPx = 7, DAC12_xDAT = 0FFFh			150	250	
		R_{Load} = 3 kΩ, 0.3 V < $V_{O/P(DAC12)}$ < AV_{CC} – 0.3 V, DAC12AMPx = 7			1	4	

(1) Data is valid after the offset calibration of the output amplifier.

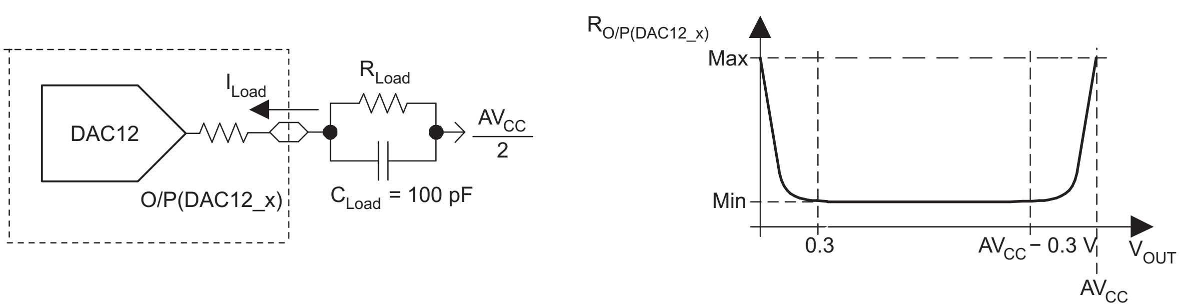


Figure 5-44. DAC12_x Output Resistance Tests

5.53 12-Bit DAC Reference Input Specifications

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
V_{eREF+}	Reference input voltage range	DAC12IR = 0 (1) (2)	2.2 V, 3 V		AV_{CC} / 3	AV_{CC} + 0.2	V
		DAC12IR = 1 (3) (4)			AV_{CC}	AV_{CC} + 0.2	
$R_{i(VREF+)}$, $R_{i(VeREF+)}$	Reference input resistance	DAC12_0 IR = DAC12_1 IR = 0	2.2 V, 3 V	20			MΩ
		DAC12_0 IR = 1, DAC12_1 IR = 0		40	48	56	kΩ
		DAC12_0 IR = 0, DAC12_1 IR = 1					
		DAC12_0 IR = DAC12_1 IR = 1, DAC12_0 SREFx = DAC12_1 SREFx (5)		20	24	28	

(1) For a full-scale output, the reference input voltage can be as high as 1/3 of the maximum output voltage swing (AV_{CC}).
(2) The maximum voltage applied at reference input voltage terminal $V_{eREF+} = [AV_{CC} – VE(O)] / [3 × (1 + E_G)]$.
(3) For a full-scale output, the reference input voltage can be as high as the maximum output voltage swing (AV_{CC}).
(4) The maximum voltage applied at reference input voltage terminal $V_{eREF+} = [AV_{CC} – V_{E(O)}] / (1 + E_G)$.
(5) When DAC12IR = 1 and DAC12SREFx = 0 or 1 for both channels, the reference input resistive dividers for each DAC are in parallel reducing the reference input resistance.

5.54 12-Bit DAC Dynamic Specifications

$V_{REF} = V_{CC}$, DAC12IR = 1, over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		V_{CC}	MIN	TYP	MAX	UNIT
t_{ON}	DAC12 on-time	DAC12_xDAT = 800h, $Error_{V(O)}$ < ±0.5 LSB (1) (see Figure 5-45)	DAC12AMPx = 0 → {2, 3, 4}	2.2 V, 3 V		60	120	µs
			DAC12AMPx = 0 → {5, 6}			15	30	
			DAC12AMPx = 0 → 7			6	12	
$t_{S(FS)}$	Settling time, full scale	DAC12_xDAT = 80h → F7Fh → 80h	DAC12AMPx = 2	2.2 V, 3 V		100	200	µs
			DAC12AMPx = 3, 5			40	80	
			DAC12AMPx = 4, 6, 7			15	30	
$t_{S(C-C)}$	Settling time, code to code	DAC12_xDAT = 3F8h → 408h → 3F8h BF8h → C08h → BF8h	DAC12AMPx = 2	2.2 V, 3 V		5		µs
			DAC12AMPx = 3, 5			2		
			DAC12AMPx = 4, 6, 7			1		
SR	Slew rate (2) (see Figure 5-46)	DAC12_xDAT = 80h → F7Fh → 80h	DAC12AMPx = 2	2.2 V, 3 V	0.05	0.12		V/µs
			DAC12AMPx = 3, 5		0.35	0.7		
			DAC12AMPx = 4, 6, 7		1.5	2.7		
	Glitch energy, full scale	DAC12_xDAT = 80h → F7Fh → 80h	DAC12AMPx = 2	2.2 V, 3 V		600		nV-s
			DAC12AMPx = 3, 5			150		
			DAC12AMPx = 4, 6, 7			30		
$BW_{–3dB}$	3-dB bandwidth, V_{DC} = 1.5 V, V_{AC} = 0.1 V_{PP} (see Figure 5-47)	DAC12AMPx = {2, 3, 4}, DAC12SREFx = 2, DAC12IR = 1, DAC12_xDAT = 800h		2.2 V, 3 V	40			kHz
		DAC12AMPx = {5, 6}, DAC12SREFx = 2, DAC12IR = 1, DAC12_xDAT = 800h			180			
		DAC12AMPx = 7, DAC12SREFx = 2, DAC12IR = 1, DAC12_xDAT = 800h			550			
	Channel-to-channel crosstalk (1) (see Figure 5-48)	DAC12_0DAT = 800h, No load, DAC12_1DAT = 80h ↔ F7Fh, R_{Load} = 3 kΩ, f_{DAC12_1OUT} = 10 kHz, Duty cycle = 50%		2.2 V, 3 V		–80		dB
		DAC12_0DAT = 80h ↔ F7Fh, R_{Load} = 3 kΩ, DAC12_1DAT = 800h, No load, f_{DAC12_0OUT} = 10 kHz, Duty cycle = 50%				–80		

(1) R_{Load} and C_{Load} are connected to AV_{SS} (not AV_{CC}/2) in Figure 5-45.
(2) Slew rate applies to output voltage steps ≥ 200 mV.

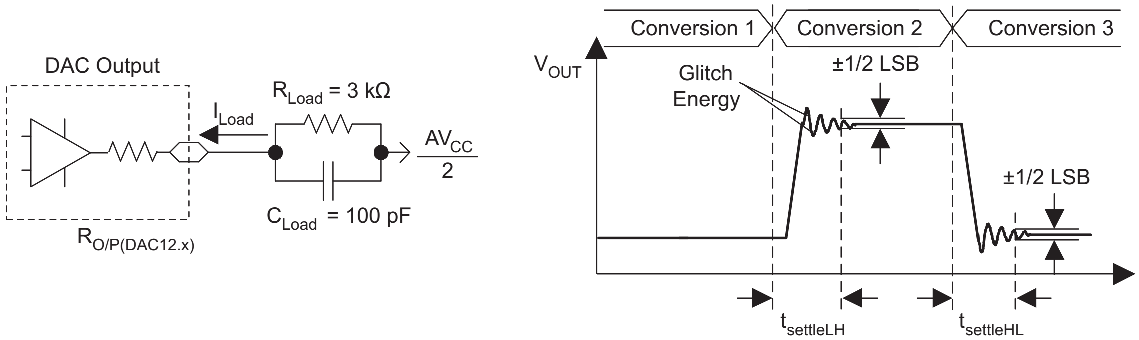


Figure 5-45. Settling Time and Glitch Energy Testing

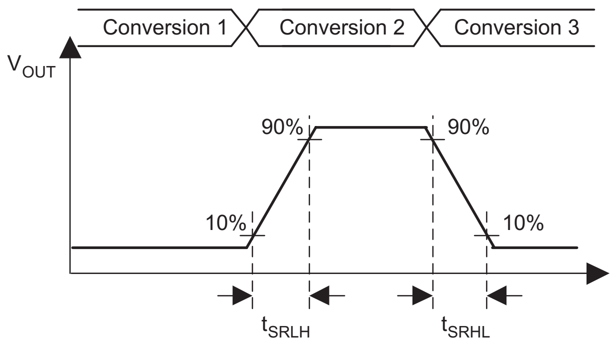


Figure 5-46. Slew Rate Testing

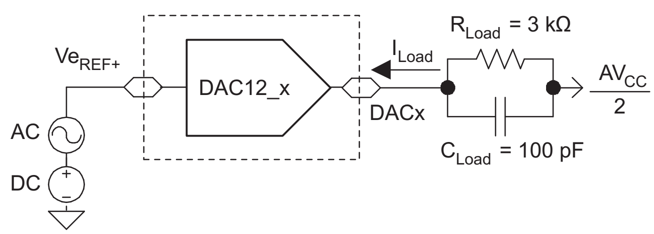


Figure 5-47. Test Conditions for 3-dB Bandwidth Specification

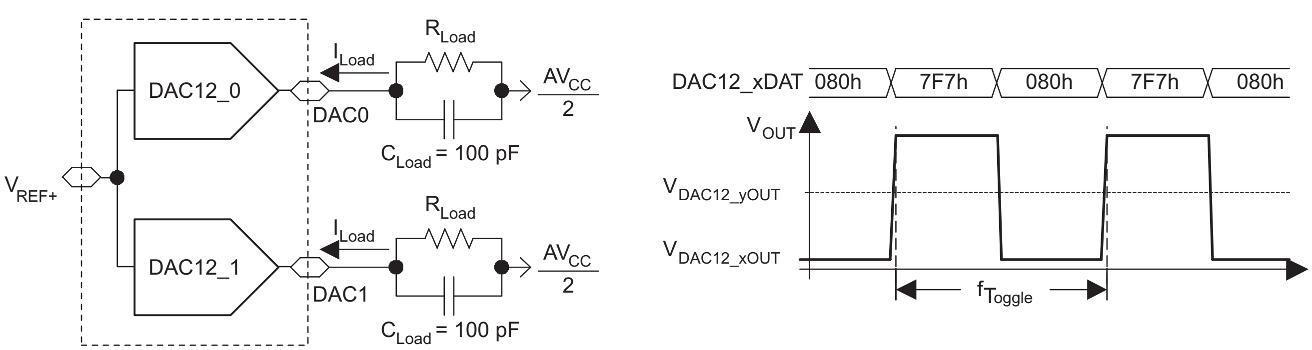


Figure 5-48. Crosstalk Test Conditions

5.55 Flash Memory

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$V_{CC(PGM/ERASE)}$	Program and erase supply voltage			2.2		3.6	V
f_{FTG}	Flash timing generator frequency			257		476	kHz
I_{PGM}	Supply current from V_{CC} during program		2.2 V/3.6 V		1	5	mA
I_{ERASE}	Supply current from V_{CC} during erase		2.2 V/3.6 V		1	7	mA
t_{CPT}	Cumulative program time (1)		2.2 V/3.6 V			10	ms
$t_{CMErase}$	Cumulative mass erase time		2.2 V/3.6 V	20			ms
	Program and erase endurance			10^4	10^5		cycles
$t_{Retention}$	Data retention duration	T_J = 25°C		100			years
t_{Word}	Word or byte program time	(2)			30		t_{FTG}
$t_{Block, 0}$	Block program time for first byte or word	(2)			25		t_{FTG}
$t_{Block, 1-63}$	Block program time for each additional byte or word	(2)			18		t_{FTG}
$t_{Block, End}$	Block program end-sequence wait time	(2)			6		t_{FTG}
$t_{Mass Erase}$	Mass erase time	(2)			10593		t_{FTG}
$t_{Seg Erase}$	Segment erase time	(2)			4819		t_{FTG}

(1) The cumulative program time must not be exceeded when writing to a 64-byte flash block. This parameter applies to all programming methods: individual word/byte write and block write modes.
(2) These values are hardwired into the state machine of the flash controller ($t_{FTG} = 1/f_{FTG}$).

5.56 RAM

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
$V_{(RAMh)}$	RAM retention supply voltage (1)	CPU halted	1.6		V

(1) This parameter defines the minimum supply voltage V_{CC} when the data in RAM remains unchanged. No program execution should happen during this supply voltage condition.

5.57 JTAG Interface

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		V_{CC}	MIN	TYP	MAX	UNIT
f_{TCK}	TCK input frequency (1)	2.2 V	0		5	MHz
		3 V	0		10	
$R_{Internal}$	Internal pullup resistance on TMS, TCK, and TDI/TCLK (2)	2.2 V, 3 V	25	60	90	kΩ

(1) f_{TCK} may be restricted to meet the timing requirements of the module selected.
(2) TMS, TCK, and TDI/TCLK pullup resistors are implemented in all versions.

5.58 JTAG Fuse (1)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		T_A	MIN	MAX	UNIT
$V_{CC(FB)}$	Supply voltage during fuse-blow condition	25°C	2.5		V
V_{FB}	Voltage level on TEST for fuse blow		6	7	V
I_{FB}	Supply current into TEST during fuse blow			100	mA
t_{FB}	Time to blow fuse			1	ms

(1) When the fuse is blown, no further access to the JTAG/Test and emulation feature is possible, and JTAG is switched to bypass mode.

6 Detailed Description

6.1 CPU

The MSP430 CPU has a 16-bit RISC architecture that is highly transparent to the application. All operations, other than program-flow instructions, are performed as register operations in conjunction with seven addressing modes for source operand and four addressing modes for destination operand.

The CPU is integrated with 16 registers that provide reduced instruction execution time. The register-to-register operation execution time is one cycle of the CPU clock.

Four of the registers, R0 to R3, are dedicated as program counter, stack pointer, status register, and constant generator respectively. The remaining registers are general-purpose registers (see Figure 6-1).

Peripherals are connected to the CPU using data, address, and control buses. Peripherals can be manged with all instructions.

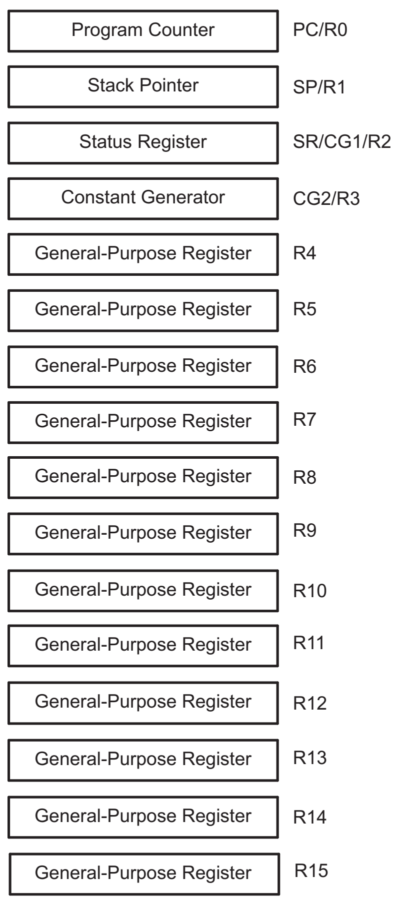


Figure 6-1. CPU Registers

6.2 Instruction Set

The instruction set consists of 51 instructions with three formats and seven address modes. Each instruction can operate on word and byte data. Table 6-1 lists examples of the three types of instruction formats; Table 6-2 lists the address modes.

Table 6-1. Instruction Word Formats

INSTRUCTION FORMAT	EXAMPLE	OPERATION
Dual operands, source and destination	ADD R4,R5	R4 + R5 → R5
Single operands, destination only	CALL R8	PC → (TOS), R8 → PC
Relative jump, unconditional or conditional	JNE	Jump-on-equal bit = 0

Table 6-2. Address Mode Descriptions

ADDRESS MODE	S (1)	D (1)	SYNTAX	EXAMPLE	OPERATION
Register	✓	✓	MOV Rs,Rd	MOV R10,R11	R10 → R11
Indexed	✓	✓	MOV X(Rn),Y(Rm)	MOV 2(R5),6(R6)	M(2+R5) → M(6+R6)
Symbolic (PC relative)	✓	✓	MOV EDE,TONI		M(EDE) → M(TONI)
Absolute	✓	✓	MOV &MEM,&TCDAT		M(MEM) → M(TCDAT)
Indirect	✓		MOV @Rn,Y(Rm)	MOV @R10,Tab(R6)	M(R10) → M(Tab+R6)
Indirect autoincrement	✓		MOV @Rn+,Rm	MOV @R10+,R11	M(R10) → R11 R10 + 2 → R10
Immediate	✓		MOV #X,TONI	MOV #45,TONI	#45 → M(TONI)

(1) S = source, D = destination

6.3 Operating Modes

The MSP430 has one active mode and five software-selectable low-power modes of operation. An interrupt event can wake the device from any of the five low-power modes, service the request, and restore back to the low-power mode on return from the interrupt program.

The following six operating modes can be configured by software:

- Active mode (AM)
  - All clocks are active
- Low-power mode 0 (LPM0)
  - CPU is disabled
  - ACLK and SMCLK remain active
  - MCLK is disabled
- Low-power mode 1 (LPM1)
  - CPU is disabled
  - ACLK and SMCLK remain active. MCLK is disabled
  - DC generator of the DCO is disabled if DCO not used in active mode
- Low-power mode 2 (LPM2)
  - CPU is disabled
  - MCLK and SMCLK are disabled
  - DC generator of the DCO remains enabled
  - ACLK remains active
- Low-power mode 3 (LPM3)
  - CPU is disabled
  - MCLK and SMCLK are disabled
  - DC generator of the DCO is disabled
  - ACLK remains active
- Low-power mode 4 (LPM4)
  - CPU is disabled
  - ACLK is disabled
  - MCLK and SMCLK are disabled
  - DC generator of the DCO is disabled
  - Crystal oscillator is stopped

6.4 Interrupt Vector Addresses

The interrupt vectors and the power up starting address are in the address range of 0FFFFh to 0FFC0h. The vector contains the 16-bit address of the appropriate interrupt handler instruction sequence.

If the reset vector (at address 0FFFEh) contains 0FFFFh (for example, flash is not programmed) the CPU enters LPM4 immediately after power up.

Table 6-3. Interrupt Sources

INTERRUPT SOURCE	INTERRUPT FLAG	SYSTEM INTERRUPT	WORD ADDRESS	PRIORITY
Power up External reset Watchdog Timer+ Flash key violation PC out of range(1)	PORIFG RSTIFG WDTIFG KEYV See (2)	Reset	0FFFEh	31, highest
NMI Oscillator fault Flash memory access violation	NMIIFG OFIFG ACCVIFG(2)(3)	(Non)maskable, (Non)maskable, (Non)maskable	0FFFCh	30
Timer_B7	TBCCR0 CCIFG(4)	Maskable	0FFFAh	29
Timer_B7	TBCCR1 to TBCCR6 CCIFGs, TBIFG(2)(4)	Maskable	0FFF8h	28
Comparator_A+	CAIFG	Maskable	0FFF6h	27
Watchdog Timer+	WDTIFG	Maskable	0FFF4h	26
Timer_A3	TACCR0 CCIFG(4)	Maskable	0FFF2h	25
Timer_A3	TACCR1 CCIFG TACCR2 CCIFG(2)(4)	Maskable	0FFF0h	24
USCI_A0 or USCI_B0 receive USCI_B0 I^2C status	UCA0RXIFG, UCB0RXIFG(2)(5)	Maskable	0FFEEh	23
USCI_A0 or USCI_B0 transmit USCI_B0 I^2C receive or transmit	UCA0TXIFG, UCB0TXIFG(2)(6)	Maskable	0FFECh	22
ADC12	ADC12IFG(2)(4)	Maskable	0FFEAh	21
			0FFE8h	20
I/O port P2 (eight flags)	P2IFG.0 to P2IFG.7(2)(4)	Maskable	0FFE6h	19
I/O port P1 (eight flags)	P1IFG.0 to P1IFG.7(2)(4)	Maskable	0FFE4h	18
USCI_A1 or USCI_B1 receive USCI_B1 I^2C status	UCA1RXIFG, UCB1RXIFG(2)(5)	Maskable	0FFE2h	17
USCI_A1 or USCI_B1 transmit USCI_B1 I^2C receive or transmit	UCA1TXIFG, UCB1TXIFG(2)(6)	Maskable	0FFE0h	16
DMA	DMA0IFG, DMA1IFG, DMA2IFG(2)(4)	Maskable	0FFDEh	15
DAC12	DAC12_0IFG, DAC12_1IFG(2)(4)	Maskable	0FFDCh	14
See (7)(8)			0FFDAh to 0FFC0h	15 to 0, lowest

(1) A reset is generated if the CPU tries to fetch instructions from within the module register memory address range (0h to 01FFh) or from within unused address ranges.
(2) Multiple source flags
(3) (Non)maskable: the individual interrupt-enable bit can disable an interrupt event, but the general interrupt enable cannot.
(4) Interrupt flags are in the module.
(5) In SPI mode: UCB0RXIFG. In I^2C mode: UCALIFG, UCNACKIFG, ICSTTIFG, UCSTPIFG.
(6) In UART or SPI mode: UCB0TXIFG. In I^2C mode: UCB0RXIFG, UCB0TXIFG.
(7) The address 0FFBEh is used as bootloader security key (BSLSKEY).
A 0AA55h at this location disables the BSL completely.
A zero disables the erasure of the flash if an invalid password is supplied.
(8) The interrupt vectors at addresses 0FFDAh to 0FFC0h are not used in this device and can be used for regular program code if necessary.

6.5 Special Function Registers (SFRs)

Most interrupt and module enable bits are collected into the lowest address space. Special function register bits not allocated to a functional purpose are not physically present in the device. Simple software access is provided with this arrangement.

Legend

rw	Bit can be read and written.
rw-0, rw-1	Bit can be read and written. It is Reset or Set by PUC.
rw-(0), rw-(1)	Bit can be read and written. It is Reset or Set by POR.
(shaded)	SFR bit is not present in device.

Figure 6-2. Interrupt Enable Register 1 (Address = 00h)

7	6	5	4	3	2	1	0
		ACCVIE	NMIIE			OFIE	WDTIE
		rw-0	rw-0			rw-0	rw-0

Table 6-4. Interrupt Enable Register 1 Description

BIT	FIELD	TYPE	RESET	DESCRIPTION
5	ACCVIE	RW	0h	Flash access violation interrupt enable
4	NMIIE	RW	0h	(Non)maskable interrupt enable
1	OFIE	RW	0h	Oscillator fault interrupt enable
0	WDTIE	RW	0h	Watchdog timer interrupt enable. Inactive if watchdog mode is selected. Active if the watchdog timer is configured in interval timer mode.

Figure 6-3. Interrupt Enable Register 2 (Address = 01h)

7	6	5	4	3	2	1	0
				UCB0TXIE	UCB0RXIE	UCA0TXIE	UCA0RXIE
				rw-0	rw-0	rw-0	rw-0

Table 6-5. Interrupt Enable Register 2 Description

BIT	FIELD	TYPE	RESET	DESCRIPTION
3	UCB0TXIE	RW	0h	USCI_B0 transmit interrupt enable
2	UCB0RXIE	RW	0h	USCI_B0 receive interrupt enable
1	UCA0TXIE	RW	0h	USCI_A0 transmit interrupt enable
0	UCA0RXIE	RW	0h	USCI_A0 receive interrupt enable

Figure 6-4. Interrupt Flag Register 1 (Address = 02h)

7	6	5	4	3	2	1	0
			NMIIFG	RSTIFG	PORIFG	OFIFG	WDTIFG
			rw-0	rw-(0)	rw-(1)	rw-1	rw-(0)

Table 6-6. Interrupt Flag Register 1 Description

BIT	FIELD	TYPE	RESET	DESCRIPTION
4	NMIIFG	RW	0h	Set by the $\overline{RST}$/NMI pin
3	RSTIFG	RW	0h	External reset interrupt flag. Set on a reset condition at $\overline{RST}$/NMI pin in reset mode. Reset on V_{CC} power up.
2	PORIFG	RW	1h	Power-on reset interrupt flag. Set on V_{CC} power up.
1	OFIFG	RW	1h	Flag set on oscillator fault.
0	WDTIFG	RW	0h	Set on watchdog timer overflow (in watchdog mode) or security key violation. Reset on V_{CC} power on or a reset condition at the $\overline{RST}$/NMI pin in reset mode.

Figure 6-5. Interrupt Flag Register 2 (Address = 03h)

7	6	5	4	3	2	1	0
				UCB0TXIFG	UCB0RXIFG	UCA0TXIFG	UCA0RXIFG
				rw-1	rw-0	rw-1	rw-0

Table 6-7. Interrupt Flag Register 2 Description

BIT	FIELD	TYPE	RESET	DESCRIPTION
3	UCB0TXIFG	RW	0h	USCI_B0 transmit interrupt flag
2	UCB0RXIFG	RW	1h	USCI_B0 receive interrupt flag
1	UCA0TXIFG	RW	1h	USCI_A0 transmit interrupt flag
0	UCA0RXIFG	RW	0h	USCI_A0 receive interrupt flag

6.6 Memory Organization

Table 6-8 summarizes the memory map of each device variant.

Table 6-8. Memory Organization

		MSP430F2416 MSP430F2616	MSP430F2417 MSP430F2617	MSP430F2418 MSP430F2618	MSP430F2419 MSP430F2619
Memory	Size	92KB	92KB	116KB	120KB
Main: interrupt vector	Flash	0x0FFFF to 0x0FFC0	0x0FFFF to 0x0FFC0	0x0FFFF to 0x0FFC0	0x0FFFF to 0x0FFC0
Main: code memory	Flash	0x18FFF to 0x02100	0x19FFF to 0x03100	0x1FFFF to 0x03100	0x1FFFF to 0x02100
RAM (total)	Size	4KB 0x020FF to 0x01100	8KB 0x030FF to 0x01100	8KB 0x030FF to 0x01100	4KB 0x020FF to 0x01100
Extended	Size	2KB 0x020FF to 0x01900	6KB 0x030FF to 0x01900	6KB 0x030FF to 0x01900	2KB 0x020FF to 0x01900
Mirrored	Size	2KB 0x018FF to 0x01100	2KB 0x018FF to 0x01100	2KB 0x018FF to 0x01100	2KB 0x018FF to 0x01100
Information memory	Size	256 bytes	256 bytes	256 bytes	256 bytes
	Info A	0x010FF to 0x010C0	0x010FF to 0x010C0	0x010FF to 0x010C0	0x010FF to 0x010C0
	Info B	0x010BF to 0x01080	0x010BF to 0x01080	0x010BF to 0x01080	0x010BF to 0x01080
	Info C	0x0107F to 0x01040	0x0107F to 0x01040	0x0107F to 0x01040	0x0107F to 0x01040
	Info D	0x0103F to 0x01000	0x0103F to 0x01000	0x0103F to 0x01000	0x0103F to 0x01000
Boot memory	Size	1KB	1KB	1KB	1KB
	ROM	0x00FFF to 0x00C00	0x00FFF to 0x00C00	0x00FFF to 0x00C00	0x00FFF to 0x00C00
RAM (mirrored at 0x18FF to 0x01100)	Size	2KB 0x009FF to 0x00200	2KB 0x009FF to 0x00200	2KB 0x009FF to 0x00200	2KB 0x009FF to 0x00200
Peripherals	16-bit	0x001FF to 0x00100	0x001FF to 0x00100	0x001FF to 0x00100	0x001FF to 0x00100
	8-bit	0x000FF to 0x00010	0x000FF to 0x00010	0x000FF to 0x00010	0x000FF to 0x00010
	8-bit SFR	0x0000F to 0x00000	0x0000F to 0x00000	0x0000F to 0x00000	0x0000F to 0x00000

6.7 Bootloader (BSL)

The MSP430 BSL lets users program the flash memory or RAM using a UART serial interface. Table 6-9 lists the BSL pin requirements. Access to the MSP430 memory through the BSL is protected by a user-defined password. For complete description of the features of the BSL and its implementation, see the *MSP430™ Flash Devices Bootloader (BSL) User's Guide*.

Table 6-9. BSL Pin Functions

BSL FUNCTION	PM, PN PACKAGE PINS	ZCA, ZQW PACKAGE PINS
Data Transmit	13 - P1.1	H1 - P1.1
Data Receive	22 - P2.2	M3 - P2.2

6.8 Flash Memory

The flash memory can be programmed via the JTAG port, the bootloader, or in-system by the CPU. The CPU can perform single-byte and single-word writes to the flash memory. Features of the flash memory include:

- Flash memory has n segments of main memory and four segments of information memory (A to D) of 64 bytes each. Each segment in main memory is 512 bytes in size.
- Segments 0 to n may be erased in one step, or each segment may be individually erased.
- Segments A to D can be erased individually, or as a group with segments 0 to n. Segments A to D are also called *information memory.*

- Segment A contains calibration data. After reset segment A is protected against programming and erasing. It can be unlocked but care should be taken not to erase this segment if the device-specific calibration data is required.
- Flash content integrity check with marginal read modes

6.9 Peripherals

Peripherals are connected to the CPU through data, address, and control buses and can be handled using all instructions. For complete module descriptions, see the *MSP430F2xx, MSP430G2xx Family User's Guide*.

6.9.1 DMA Controller (MSP430F261x Only)

The DMA controller allows movement of data from one memory address to another without CPU intervention. For example, the DMA controller can be used to move data from the ADC12 conversion memory to RAM. Using the DMA controller can increase the throughput of peripheral modules. The DMA controller reduces system power consumption by allowing the CPU to remain in sleep mode without having to awaken to move data to or from a peripheral.

6.9.2 Oscillator and System Clock

The clock system in the MSP430F241x and MSP430F261x family of devices is supported by the basic clock module that includes support for a 32768-Hz watch crystal oscillator, an internal very low-power low-frequency oscillator, an internal digitally controlled oscillator (DCO), and a high-frequency crystal oscillator. The basic clock module is designed to meet the requirements of both low system cost and low power consumption. The internal DCO provides a fast turnon clock source and stabilizes in less than 1 µs. The basic clock module provides the following clock signals:

- Auxiliary clock (ACLK), sourced either from a 32768-Hz watch crystal or the internal LF oscillator.
- Main clock (MCLK), the system clock used by the CPU.
- Sub-Main clock (SMCLK), the subsystem clock used by the peripheral modules.

The DCO settings to calibrate the DCO output frequency are stored in the information memory segment A.

6.9.3 Calibration Data Stored in Information Memory Segment A

Calibration data is stored for the DCO and for the ADC12. It is organized in a tag-length-value (TLV) structure (see Table 6-10 and Table 6-11).

Table 6-10. Tags Used by the TLV Structure

NAME	ADDRESS	VALUE	DESCRIPTION
TAG_DCO_30	0x10F6	0x01	DCO frequency calibration at V_{CC} = 3 V and T_A = 25°C
TAG_ADC12_1	0x10DA	0x08	ADC12_1 calibration tag
TAG_EMPTY	–	0xFE	Identifier for empty memory areas

Table 6-11. Labels Used by the ADC Calibration Structure

LABEL	ADDRESS OFFSET	SIZE	CONDITION AT CALIBRATION
CAL_ADC_25T85	0x0010	Word	INCHx = 1010b, REF2_5 = 1, T_A = 85°C
CAL_ADC_25T30	0x000E	Word	INCHx = 1010b, REF2_5 = 1, T_A = 30°C
CAL_ADC_25VREF_FACTOR	0x000C	Word	REF2_5 = 1, T_A = 30°C
CAL_ADC_15T85	0x000A	Word	INCHx = 1010b, REF2_5 = 0, T_A = 85°C
CAL_ADC_15T30	0x0008	Word	INCHx = 1010b, REF2_5 = 0, T_A = 30°C
CAL_ADC_15VREF_FACTOR	0x0006	Word	REF2_5 = 0, T_A = 30°C
CAL_ADC_OFFSET	0x0004	Word	External V_{REF} = 1.5 V, $f_{ADC12CLK}$ = 5 MHz
CAL_ADC_GAIN_FACTOR	0x0002	Word	External V_{REF} = 1.5 V, $f_{ADC12CLK}$ = 5 MHz
CAL_BC1_1MHZ	0x0009	Byte	–
CAL_DCO_1MHZ	0x0008	Byte	–
CAL_BC1_8MHZ	0x0007	Byte	–
CAL_DCO_8MHZ	0x0006	Byte	–
CAL_BC1_12MHZ	0x0005	Byte	–
CAL_DCO_12MHZ	0x0004	Byte	–
CAL_BC1_16MHZ	0x0003	Byte	–
CAL_DCO_16MHZ	0x0002	Byte	–

6.9.4 Brownout, Supply Voltage Supervisor (SVS)

The brownout circuit is implemented to provide the proper internal reset signal to the device during power on and power off. The SVS circuitry detects if the supply voltage drops below a user selectable level and supports both supply voltage supervision (the device is automatically reset) and supply voltage monitoring (SVM) (the device is not automatically reset).

The CPU begins code execution after the brownout circuit releases the device reset. However, V_{CC} may not have ramped to $V_{CC(min)}$ at that time. The user must ensure that the default DCO settings are not changed until V_{CC} reaches $V_{CC(min)}$. If desired, the SVS circuit can be used to determine when V_{CC} reaches $V_{CC(min)}$.

6.9.5 Digital I/O

Up to eight 8-bit I/O ports are implemented—ports P1 to P8:

- All individual I/O bits are independently programmable.
- Any combination of input, output, and interrupt condition is possible.
- Edge-selectable interrupt input capability for all 8 bits of both port P1 and port P2.
- Read and write access to port-control registers is supported by all instructions.
- Each I/O has an individually programmable pullup or pulldown resistor.
- Ports P7 and P8 can be accessed word-wise.

6.9.6 Watchdog Timer (WDT+)

The primary function of the WDT+ module is to perform a controlled system restart after a software problem occurs. If the selected time interval expires, a system reset is generated. If the watchdog function is not needed in an application, the module can be disabled or configured as an interval timer and can generate interrupts at selected time intervals.

6.9.7 Hardware Multiplier

The multiplication operation is supported by a dedicated peripheral module. The module performs 16- × 16-bit, 16- × 8-bit, 8- × 16-bit, and 8- × 8-bit operations. The module supports signed and unsigned multiplication as well as signed and unsigned multiply-and-accumulate operations. The result of an operation can be accessed immediately after the operands have been loaded into the peripheral registers. No additional clock cycles are required.

6.9.8 Universal Serial Communication Interface (USCI)

The USCI modules are used for serial data communication. The USCI module supports synchronous communication protocols such as SPI (3-pin or 4-pin) or I^2C, and asynchronous combination protocols such as UART, enhanced UART with automatic baudrate detection (LIN), and IrDA.

The USCI_A module provides support for SPI (3-pin or 4-pin), UART, enhanced UART, and IrDA.

The USCI_B module provides support for SPI (3-pin or 4-pin) and I^2C

6.9.9 Timer_A3

Timer_A3 is a 16-bit timer/counter with three capture/compare registers. Timer_A3 supports multiple capture/compares, PWM outputs, and interval timing (see Table 6-12). Timer_A3 also has extensive interrupt capabilities. Interrupts may be generated from the counter on overflow conditions and from each of the capture/compare registers.

Table 6-12. Timer_A3 Signal Connections

INPUT PIN NUMBER		DEVICE INPUT SIGNAL	MODULE INPUT NAME	MODULE BLOCK	MODULE OUTPUT SIGNAL	OUTPUT PIN NUMBER	
ZCA, ZQW	PM, PN					PM, PN	ZCA, ZQW
G2 - P1.0	12 - P1.0	TACLK	TACLK	Timer	NA		
		ACLK	ACLK				
		SMCLK	SMCLK				
M2 - P2.1	21 - P2.1	TAINCLK	INCLK				
H1 - P1.1	13 - P1.1	TA0	CCI0A	CCR0	TA0	13 - P1.1	H1 - P1.1
M3 - P2.2	22 - P2.2	TA0	CCI0B			17 - P1.5	K1 - P1.5
		DV_{SS}	GND			27 - P2.7	L5 - P2.7
		DV_{CC}	V_{CC}				
H2 - P1.2	14 - P1.2	TA1	CCI1A	CCR1	TA1	14 - P1.2	H2 - P1.2
		CAOUT (internal)	CCI1B			18 - P1.6	K2 - P1.6
		DV_{SS}	GND			23 - P2.3	L3 - P2.3
		DV_{CC}	V_{CC}			ADC12 (internal)	
						DAC12_0 (internal)	
						DAC12_1 (internal)	
J1 - P1.3	15 - P1.3	TA2	CCI2A	CCR2	TA2	15 - P1.3	J1 - P1.3
		ACLK (internal)	CCI2B			19 - P1.7	L1 - P1.7
		DV_{SS}	GND			24 - P2.4	L4 - P2.4
		DV_{CC}	V_{CC}				

6.9.10 Timer_B7

Timer_B7 is a 16-bit timer/counter with seven capture/compare registers. Timer_B7 supports multiple capture/compares, PWM outputs, and interval timing (see Table 6-13). Timer_B7 also has extensive interrupt capabilities. Interrupts may be generated from the counter on overflow conditions and from each of the capture/compare registers.

Table 6-13. Timer_B3, Timer_B7 Signal Connections

INPUT PIN NUMBER		DEVICE INPUT SIGNAL	MODULE INPUT NAME	MODULE BLOCK	MODULE OUTPUT SIGNAL	OUTPUT PIN NUMBER	
ZCA, ZQW	PM, PN					PM, PN	ZCA, ZQW
K11 - P4.7	43 - P4.7	TBCLK	TBCLK	Timer	NA		
		ACLK	ACLK				
		SMCLK	SMCLK				
K11 - P4.7	43 - P4.7	TBCLK	INCLK				
M9 - P4.0	36 - P4.0	TB0	CCI0A	CCR0	TB0	36 - P4.0	M9 - P4.0
M9- P4.0	36 - P4.0	TB0	CCI0B			ADC12 (internal)	
		DV_{SS}	GND				
		DV_{CC}	V_{CC}				
J9 - P4.1	37 - P4.1	TB1	CCI1A	CCR1	TB1	37 - P4.1	J9 - P4.1
J9 - P4.1	37 - P4.1	TB1	CCI1B			ADC12 (internal)	
		DV_{SS}	GND				
		DV_{CC}	V_{CC}				
M10 - P4.2	38 - P4.2	TB2	CCI2A	CCR2	TB2	38 - P4.2	M10 - P4.2
M10 - P4.2	38 - P4.2	TB2	CCI2B			DAC_0 (internal)	
		DV_{SS}	GND			DAC_1 (internal)	
		DV_{CC}	V_{CC}				
L10 - P4.3	39 - P4.3	TB3	CCI3A	CCR3	TB3	39 - P4.3	L10 - P4.3
L10 - P4.3	39 - P4.3	TB3	CCI3B				
		DV_{SS}	GND				
		DV_{CC}	V_{CC}				
M11 - P4.4	40 - P4.4	TB4	CCI4A	CCR4	TB4	40 - P4.4	M11 - P4.4
M11 - P4.4	40 - P4.4	TB4	CCI4B				
		DV_{SS}	GND				
		DV_{CC}	V_{CC}				
M12 - P4.5	41 - P4.5	TB5	CCI5A	CCR5	TB5	41 - P4.5	M12 - P4.5
M12 - P4.5	41 - P4.5	TB5	CCI5B				
		DV_{SS}	GND				
		DV_{CC}	V_{CC}				
L12 - P4.6	42 - P4.6	TB6	CCI6A	CCR6	TB6	42 - P4.6	L12 - P4.6
		ACLK (internal)	CCI6B				
		DV_{SS}	GND				
		DV_{CC}	V_{CC}				

6.9.11 Comparator_A+

The primary function of the Comparator_A+ module is to support precision slope analog-to-digital conversions, battery-voltage supervision, and monitoring of external analog signals.

6.9.12 ADC12

The ADC12 module supports fast 12-bit analog-to-digital conversions. The module implements a 12-bit SAR core, sample select control, reference generator, and a 16-word conversion-and-control buffer. The conversion-and-control buffer allows the conversion and storage of up to 16 independent ADC samples without any CPU intervention.

6.9.13 DAC12 (MSP430F261x Only)

The DAC12 module is a 12-bit R-ladder voltage-output digital-to-analog converter (DAC). The DAC12 may be used in 8-bit or 12-bit mode and may be used with the DMA controller. When multiple DAC12 modules are present, they may be grouped together for synchronous operation.

6.9.14 Peripheral File Map

Table 6-14 lists the supported registers for each peripheral module.

Table 6-14. Peripherals File Map

MODULE	REGISTER	ACRONYM	ADDRESS
DMA[(1)]	DMA channel 2 transfer size	DMA2SZ	0x01F2
	DMA channel 2 destination address	DMA2DA	0x01EE
	DMA channel 2 source address	DMA2SA	0x01EA
	DMA channel 2 control	DMA2CTL	0x01E8
	DMA channel 1 transfer size	DMA1SZ	0x01E6
	DMA channel 1 destination address	DMA1DA	0x01E2
	DMA channel 1 source address	DMA1SA	0x01DE
	DMA channel 1 control	DMA1CTL	0x01DC
	DMA channel 0 transfer size	DMA0SZ	0x01DA
	DMA channel 0 destination address	DMA0DA	0x01D6
	DMA channel 0 source address	DMA0SA	0x01D2
	DMA channel 0 control	DMA0CTL	0x01D0
	DMA module interrupt vector word	DMAIV	0x0126
	DMA module control 1	DMACTL1	0x0124
	DMA module control 0	DMACTL0	0x0122
DAC12[(1)]	DAC12_1 data	DAC12_1DAT	0x01CA
	DAC12_1 control	DAC12_1CTL	0x01C2
	DAC12_0 data	DAC12_0DAT	0x01C8
	DAC12_0 control	DAC12_0CTL	0x01C0

(1) MSP430F261x devices only

Table 6-14. Peripherals File Map (continued)

MODULE	REGISTER	ACRONYM	ADDRESS
ADC12	Interrupt vector word	ADC12IV	0x01A8
	Interrupt enable	ADC12IE	0x01A6
	Interrupt flag	ADC12IFG	0x01A4
	Control 1	ADC12CTL1	0x01A2
	Control 0	ADC12CTL0	0x01A0
	Conversion memory 15	ADC12MEM15	0x015E
	Conversion memory 14	ADC12MEM14	0x015C
	Conversion memory 13	ADC12MEM13	0x015A
	Conversion memory 12	ADC12MEM12	0x0158
	Conversion memory 11	ADC12MEM11	0x0156
	Conversion memory 10	ADC12MEM10	0x0154
	Conversion memory 9	ADC12MEM9	0x0152
	Conversion memory 8	ADC12MEM8	0x0150
	Conversion memory 7	ADC12MEM7	0x014E
	Conversion memory 6	ADC12MEM6	0x014C
	Conversion memory 5	ADC12MEM5	0x014A
	Conversion memory 4	ADC12MEM4	0x0148
	Conversion memory 3	ADC12MEM3	0x0146
	Conversion memory 2	ADC12MEM2	0x0144
	Conversion memory 1	ADC12MEM1	0x0142
	Conversion memory 0	ADC12MEM0	0x0140
	ADC memory control 15	ADC12MCTL15	0x008F
	ADC memory control 14	ADC12MCTL14	0x008E
	ADC memory control 13	ADC12MCTL13	0x008D
	ADC memory control 12	ADC12MCTL12	0x008C
	ADC memory control 11	ADC12MCTL11	0x008B
	ADC memory control 10	ADC12MCTL10	0x008A
	ADC memory control 9	ADC12MCTL9	0x0089
	ADC memory control 8	ADC12MCTL8	0x0088
	ADC memory control 7	ADC12MCTL7	0x0087
	ADC memory control 6	ADC12MCTL6	0x0086
	ADC memory control 5	ADC12MCTL5	0x0085
	ADC memory control 4	ADC12MCTL4	0x0084
	ADC memory control 3	ADC12MCTL3	0x0083
	ADC memory control 2	ADC12MCTL2	0x0082
	ADC memory control 1	ADC12MCTL1	0x0081
	ADC memory control 0	ADC12MCTL0	0x0080

Table 6-14. Peripherals File Map (continued)

MODULE	REGISTER	ACRONYM	ADDRESS
Timer_B7	Capture/compare 6	TBCCR6	0x019E
	Capture/compare 5	TBCCR5	0x019C
	Capture/compare 4	TBCCR4	0x019A
	Capture/compare 3	TBCCR3	0x0198
	Capture/compare 2	TBCCR2	0x0196
	Capture/compare 1	TBCCR1	0x0194
	Capture/compare 0	TBCCR0	0x0192
	Timer_B counter	TBR	0x0190
	Capture/compare control 6	TBCCTL6	0x018E
	Capture/compare control 5	TBCCTL5	0x018C
	Capture/compare control 4	TBCCTL4	0x018A
	Capture/compare control 3	TBCCTL3	0x0188
	Capture/compare control 2	TBCCTL2	0x0186
	Capture/compare control 1	TBCCTL1	0x0184
	Capture/compare control 0	TBCCTL0	0x0182
	Timer_B control	TBCTL	0x0180
	Timer_B interrupt vector	TBIV	0x011E
Timer_A3	Capture/compare 2	TACCR2	0x0176
	Capture/compare 1	TACCR1	0x0174
	Capture/compare 0	TACCR0	0x0172
	Timer_A counter	TAR	0x0170
	Reserved		0x016E
	Reserved		0x016C
	Reserved		0x016A
	Reserved		0x0168
	Capture/compare control 2	TACCTL2	0x0166
	Capture/compare control 1	TACCTL1	0x0164
	Capture/compare control 0	TACCTL0	0x0162
	Timer_A control	TACTL	0x0160
	Timer_A interrupt vector	TAIV	0x012E
Hardware multiplier	Sum extend	SUMEXT	0x013E
	Result high word	RESHI	0x013C
	Result low word	RESLO	0x013A
	Second operand	OP2	0x0138
	Multiply signed +accumulate/operand 1	MACS	0x0136
	Multiply+accumulate/operand 1	MAC	0x0134
	Multiply signed/operand 1	MPYS	0x0132
	Multiply unsigned/operand 1	MPY	0x0130
Flash	Flash control 4	FCTL4	0x01BE
	Flash control 3	FCTL3	0x012C
	Flash control 2	FCTL2	0x012A
	Flash control 1	FCTL1	0x0128
Watchdog	Watchdog Timer control	WDTCTL	0x0120

Table 6-14. Peripherals File Map (continued)

MODULE	REGISTER	ACRONYM	ADDRESS
USCI_A0, USCI_B0	USCI_A0 auto baud rate control	UCA0ABCTL	0x005D
	USCI_A0 transmit buffer	UCA0TXBUF	0x0067
	USCI_A0 receive buffer	UCA0RXBUF	0x0066
	USCI_A0 status	UCA0STAT	0x0065
	USCI_A0 modulation control	UCA0MCTL	0x0064
	USCI_A0 baud rate control 1	UCA0BR1	0x0063
	USCI_A0 baud rate control 0	UCA0BR0	0x0062
	USCI_A0 control 1	UCA0CTL1	0x0061
	USCI_A0 control 0	UCA0CTL0	0x0060
	USCI_A0 IrDA receive control	UCA0IRRCTL	0x005F
	USCI_A0 IrDA transmit control	UCA0IRTCLT	0x005E
	USCI_B0 transmit buffer	UCB0TXBUF	0x006F
	USCI_B0 receive buffer	UCB0RXBUF	0x006E
	USCI_B0 status	UCB0STAT	0x006D
	USCI_B0 I2C Interrupt enable	UCB0CIE	0x006C
	USCI_B0 baud rate control 1	UCB0BR1	0x006B
	USCI_B0 baud rate control 0	UCB0BR0	0x006A
	USCI_B0 control 1	UCB0CTL1	0x0069
	USCI_B0 control 0	UCB0CTL0	0x0068
	USCI_B0 I2C slave address	UCB0SA	0x011A
	USCI_B0 I2C own address	UCB0OA	0x0118
USCI_A1, USCI_B1	USCI_A1 auto baud rate control	UCA1ABCTL	0x00CD
	USCI_A1 transmit buffer	UCA1TXBUF	0x00D7
	USCI_A1 receive buffer	UCA1RXBUF	0x00D6
	USCI_A1 status	UCA1STAT	0x00D5
	USCI_A1 modulation control	UCA1MCTL	0x00D4
	USCI_A1 baud rate control 1	UCA1BR1	0x00D3
	USCI_A1 baud rate control 0	UCA1BR0	0x00D2
	USCI_A1 control 1	UCA1CTL1	0x00D1
	USCI_A1 control 0	UCA1CTL0	0x00D0
	USCI_A1 IrDA receive control	UCA1IRRCTL	0x00CF
	USCI_A1 IrDA transmit control	UCA1IRTCLT	0x00CE
	USCI_B1 transmit buffer	UCB1TXBUF	0x00DF
	USCI_B1 receive buffer	UCB1RXBUF	0x00DE
	USCI_B1 status	UCB1STAT	0x00DD
	USCI_B1 I2C Interrupt enable	UCB1CIE	0x00DC
	USCI_B1 baud rate control 1	UCB1BR1	0x00DB
	USCI_B1 baud rate control 0	UCB1BR0	0x00DA
	USCI_B1 control 1	UCB1CTL1	0x00D9
	USCI_B1 control 0	UCB1CTL0	0x00D8
	USCI_B1 I2C slave address	UCB1SA	0x017E
	USCI_B1 I2C own address	UCB1OA	0x017C
	USCI_A1/B1 interrupt enable	UC1IE	0x0006
	USCI_A1/B1 interrupt flag	UC1IFG	0x0007
Comparator_A+	Comparator_A port disable	CAPD	0x005B
	Comparator_A control2	CACTL2	0x005A
	Comparator_A control1	CACTL1	0x0059

Table 6-14. Peripherals File Map (continued)

MODULE	REGISTER	ACRONYM	ADDRESS
Basic clock	Basic clock system control 3	BCSCTL3	0x0053
	Basic clock system control 2	BCSCTL2	0x0058
	Basic clock system control 1	BCSCTL1	0x0057
	DCO clock frequency control	DCOCTL	0x0056
Brownout, SVS	SVS control (reset by brownout signal)	SVSCTL	0x0055
Port PA(2)	Port PA resistor enable	PAREN	0x0014
	Port PA selection	PASEL	0x003E
	Port PA direction	PADIR	0x003C
	Port PA output	PAOUT	0x003A
	Port PA input	PAIN	0x0038
Port P8(2)	Port P8 resistor enable	P8REN	0x0015
	Port P8 selection	P8SEL	0x003F
	Port P8 direction	P8DIR	0x003D
	Port P8 output	P8OUT	0x003B
	Port P8 input	P8IN	0x0039
Port P7(2)	Port P7 resistor enable	P7REN	0x0014
	Port P7 selection	P7SEL	0x003E
	Port P7 direction	P7DIR	0x003C
	Port P7 output	P7OUT	0x003A
	Port P7 input	P7IN	0x0038
Port P6	Port P6 resistor enable	P6REN	0x0013
	Port P6 selection	P6SEL	0x0037
	Port P6 direction	P6DIR	0x0036
	Port P6 output	P6OUT	0x0035
	Port P6 input	P6IN	0x0034
Port P5	Port P5 resistor enable	P5REN	0x0012
	Port P5 selection	P5SEL	0x0033
	Port P5 direction	P5DIR	0x0032
	Port P5 output	P5OUT	0x0031
	Port P5 input	P5IN	0x0030
Port P4	Port P4 selection	P4SEL	0x001F
	Port P4 resistor enable	P4REN	0x0011
	Port P4 direction	P4DIR	0x001E
	Port P4 output	P4OUT	0x001D
	Port P4 input	P4IN	0x001C
Port P3	Port P3 resistor enable	P3REN	0x0010
	Port P3 selection	P3SEL	0x001B
	Port P3 direction	P3DIR	0x001A
	Port P3 output	P3OUT	0x0019
	Port P3 input	P3IN	0x0018

(2) 80-pin PN and 113-pin ZCA or ZQW devices only

Table 6-14. Peripherals File Map (continued)

MODULE	REGISTER	ACRONYM	ADDRESS
Port P2	Port P2 resistor enable	P2REN	0x002F
	Port P2 selection	P2SEL	0x002E
	Port P2 interrupt enable	P2IE	0x002D
	Port P2 interrupt-edge select	P2IES	0x002C
	Port P2 interrupt flag	P2IFG	0x002B
	Port P2 direction	P2DIR	0x002A
	Port P2 output	P2OUT	0x0029
	Port P2 input	P2IN	0x0028
Port P1	Port P1 resistor enable	P1REN	0x0027
	Port P1 selection	P1SEL	0x0026
	Port P1 interrupt enable	P1IE	0x0025
	Port P1 interrupt-edge select	P1IES	0x0024
	Port P1 interrupt flag	P1IFG	0x0023
	Port P1 direction	P1DIR	0x0022
	Port P1 output	P1OUT	0x0021
	Port P1 input	P1IN	0x0020
Special functions	SFR interrupt flag 2	IFG2	0x0003
	SFR interrupt flag 1	IFG1	0x0002
	SFR interrupt enable 2	IE2	0x0001
	SFR interrupt enable 1	IE1	0x0000

6.10 Port Diagrams

6.10.1 Port P1 (P1.0 to P1.7), Input/Output With Schmitt Trigger

Figure 6-6 shows the port diagram. Table 6-15 summarizes the selection of the pin function.

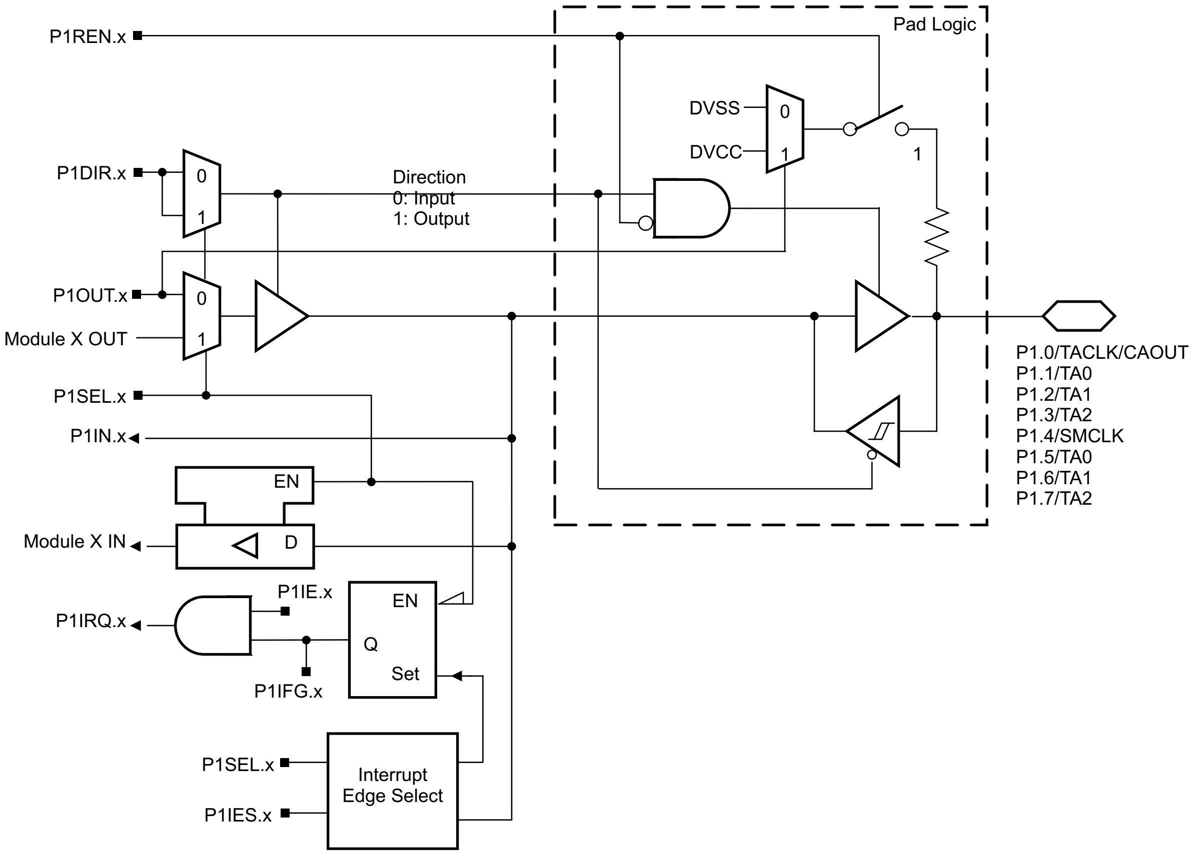


Figure 6-6. Port P1 (P1.0 to P1.7) Diagram

Table 6-15. Port P1 (P1.0 to P1.7) Pin Functions

PIN NAME (P1.x)	x	FUNCTION	CONTROL BITS OR SIGNALS	
			P1DIR.x	P1SEL.x
P1.0/TACLK/CAOUT	0	P1.0 (I/O)	0 = Input 1 = Output	0
		Timer_A3.TACLK	0	1
		CAOUT	1	1
P1.1/TA0	1	P1.1 (I/O)	0 = Input 1 = Output	0
		Timer_A3.CCI0A	0	1
		Timer_A3.TA0	1	1
P1.2/TA1	2	P1.2 (I/O)	0 = Input 1 = Output	0
		Timer_A3.CCI1A	0	1
		Timer_A3.TA1	1	1
P1.3/TA2	3	P1.3 (I/O)	0 = Input 1 = Output	0
		Timer_A3.CCI2A	0	1
		Timer_A3.TA2	1	1
P1.4/SMCLK	4	P1.4 (I/O)	0 = Input 1 = Output	0
		SMCLK	1	1
P1.5/TA0	5	P1.5 (I/O)	0 = Input 1 = Output	0
		Timer_A3.TA0	1	1
P1.6/TA1	6	P1.6 (I/O)	0 = Input 1 = Output	0
		Timer_A3.TA1	1	1
P1.7/TA2	7	P1.7 (I/O)	0 = Input 1 = Output	0
		Timer_A3.TA2	1	1

6.10.2 Port P2 (P2.0 to P2.4, P2.6, and P2.7), Input/Output With Schmitt Trigger

Figure 6-7 shows the port diagram. Table 6-16 summarizes the selection of the pin function.

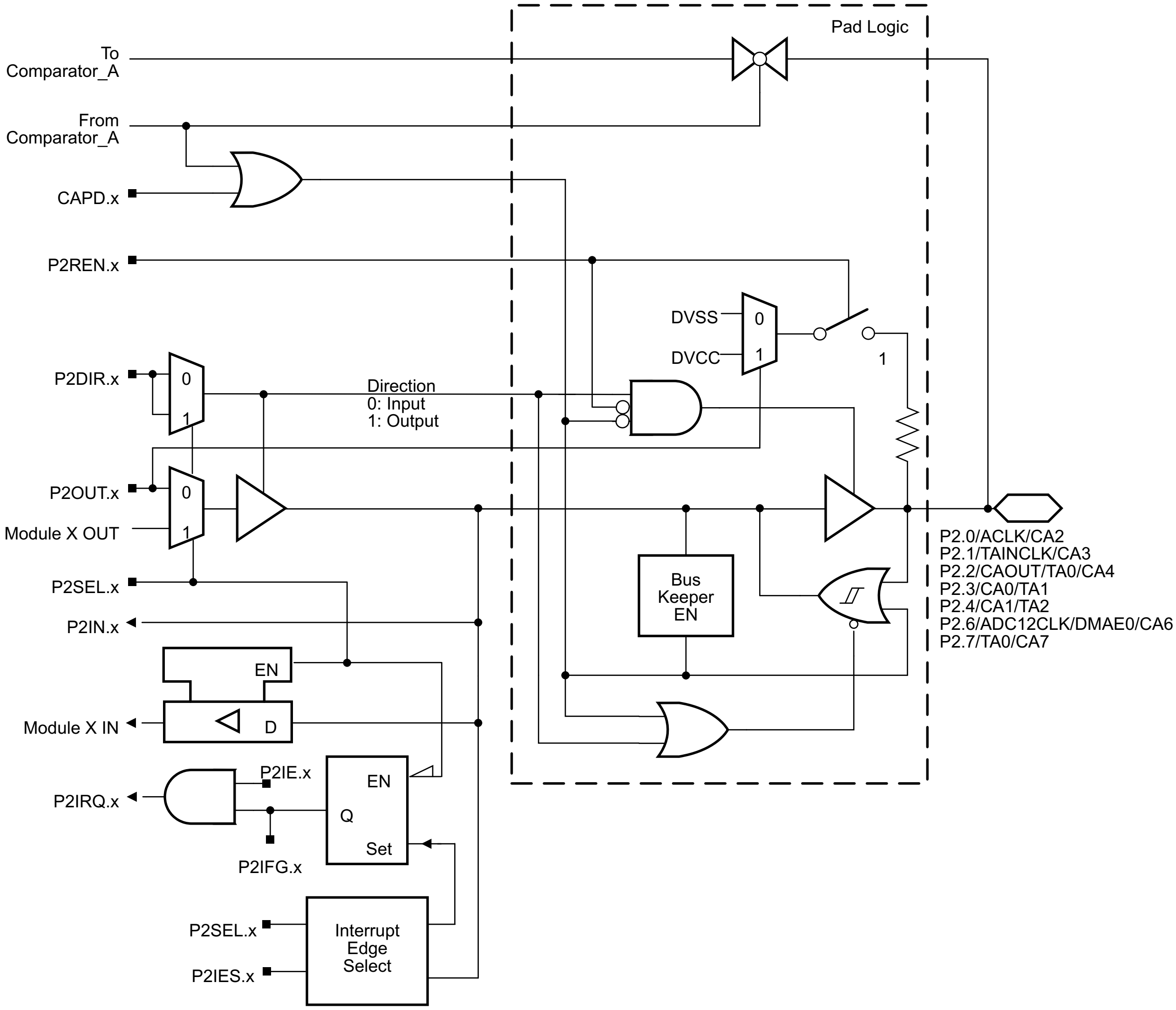


Figure 6-7. Port P2 (P2.0 to P2.4, P2.6, and P2.7) Diagram

Table 6-16. Port P2 (P2.0 to P2.4, P2.6, and P2.7) Pin Functions

PIN NAME (P2.x)	x	FUNCTION	CONTROL BITS OR SIGNALS[(1)]		
			CAPD.x	P2DIR.x	P2SEL.x
P2.0/ACLK/CA2	0	P2.0 (I/O)	0	0 = Input 1 = Output	0
		ACLK	0	1	1
		CA2	1	X	X
P2.1/TAINCLK/CA3	1	P2.1 (I/O)	0	0 = Input 1 = Output	0
		Timer_A3.INCLK	0	0	1
		DV_{SS}	0	1	1
		CA3	1	X	X
P2.2/CAOUT/TA0/CA4	2	P2.2 (I/O)	0	0 = Input 1 = Output	0
		CAOUT	0	1	1
		Timer_A3.CCI0B	0	0	1
		CA4	1	X	X
P2.3/CA0/TA1	3	P2.3 (I/O)	0	0 = Input 1 = Output	0
		Timer_A3.TA1	0	1	1
		CA0	1	X	X
P2.4/CA1/TA2	4	P2.4 (I/O)	0	0 = Input 1 = Output	0
		Timer_A3.TA2	0	1	X
		CA1	1	X	1
P2.6/ADC12CLK/ DMAE0[(2)]/CA6	6	P2.6 (I/O)	0	0 = Input 1 = Output	0
		ADC12CLK	0	1	1
		DMAE0	0	0	1
		CA6	1	X	X
P2.7/TA0/CA7	7	P2.7 (I/O)	0	0 = Input 1 = Output	0
		Timer_A3.TA0	0	1	1
		CA7	1	X	X

(1) X = Don't care
(2) MSP430F261x devices only

6.10.3 Port P2 (P2.5), Input/Output With Schmitt Trigger

Figure 6-8 shows the port diagram. Table 6-17 summarizes the selection of the pin function.

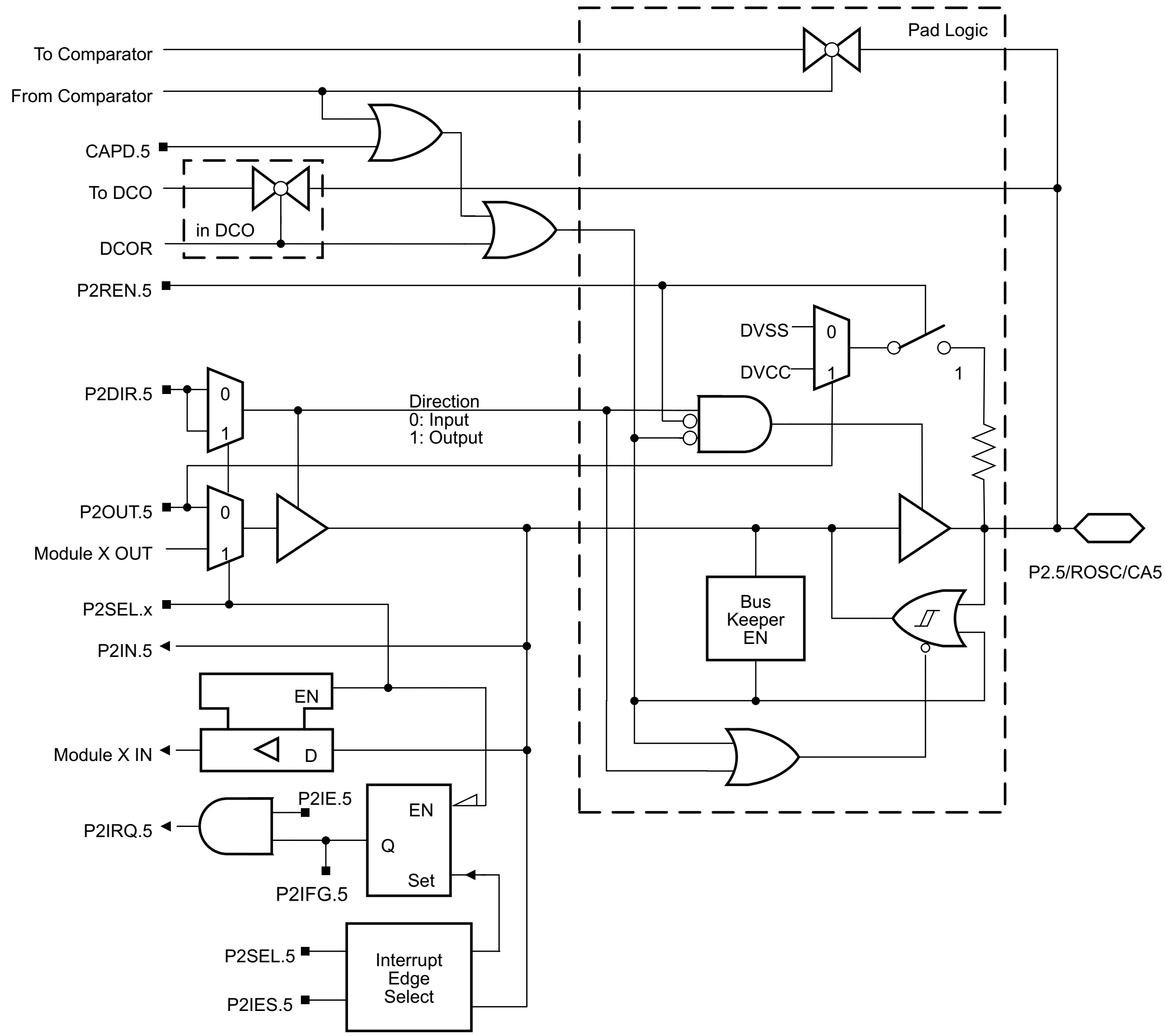


Figure 6-8. Port P2 (P2.5) Diagram

Table 6-17. Port P2 (P2.5) Pin Functions

PIN NAME (P2.x)	x	FUNCTION	CONTROL BITS OR SIGNALS(1)			
			CAPD	DCOR	P2DIR.5	P2SEL.5
P2.5/R_{OSC}/CA5	5	P2.5 (I/O)	0	0	0 = Input 1 = Output	0
		R_{OSC}(2)	0	1	X	X
		DV_{SS}	0	0	1	1
		CA5	1 or selected	0	X	X

(1) X = Don't care
(2) If R_{OSC} is used, it is connected to an external resistor.

6.10.4 Port P3 (P3.0 to P3.7), Input/Output With Schmitt Trigger

Figure 6-9 shows the port diagram. Table 6-18 summarizes the selection of the pin function.

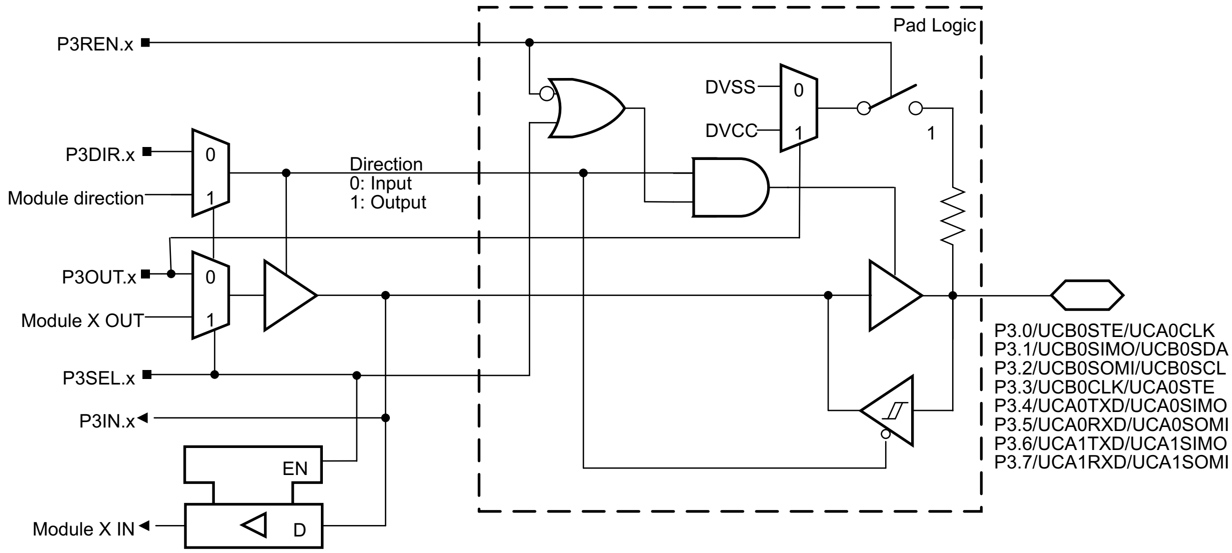


Figure 6-9. Port P3 (P3.0 to P3.7) Diagram

Table 6-18. Port P3 (P3.0 to P3.7) Pin Functions

PIN NAME (P3.x)	x	FUNCTION	CONTROL BITS OR SIGNALS (1)	
			P3DIR.x	P3SEL.x
P3.0/UCB0STE/UCA0CLK	0	P3.0 (I/O)	0 = Input 1 = Output	0
		UCB0STE/UCA0CLK (2) (3)	X	1
P3.1/UCB0SIMO/UCB0SDA	1	P3.1 (I/O)	0 = Input 1 = Output	0
		UCB0SIMO/UCB0SDA (2) (4)	X	1
P3.2/UCB0SOMI/UCB0SCL	2	P3.2 (I/O)	0 = Input 1 = Output	0
		UCB0SOMI/UCB0SCL (2) (4)	X	1
P3.3/UCB0CLK/UCA0STE	3	P3.3 (I/O)	0 = Input 1 = Output	0
		UCB0CLK/UCA0STE (2) (5)	X	1
P3.4/UCA0TXD/UCA0SIMO	4	P3.4 (I/O)	0 = Input 1 = Output	0
		UCA0TXD/UCA0SIMO (2)	X	1
P3.5/UCA0RXD/UCA0SOMI	5	P3.5 (I/O)	0 = Input 1 = Output	0
		UCA0RXD/UCA0SOMI (2)	X	1
P3.6/UCA1TXD/UCA1SIMO	6	P3.6 (I/O)	0 = Input 1 = Output	0
		UCA1TXD/UCA1SIMO (2)	X	1

(1) X = Don't care
(2) The pin direction is controlled by the USCI module.
(3) UCA0CLK function takes precedence over UCB0STE function. If the pin is required as UCA0CLK input or output, USCI_B0 is forced to 3-wire SPI mode if 4-wire SPI mode is selected.
(4) If the I²C functionality is selected, the output drives only the logical 0 to V_{SS} level.
(5) UCB0CLK function takes precedence over UCA0STE function. If the pin is required as UCB0CLK input or output, USCI_A0 is forced to 3-wire SPI mode if 4-wire SPI mode is selected.

Table 6-18. Port P3 (P3.0 to P3.7) Pin Functions (continued)

PIN NAME (P3.x)	x	FUNCTION	CONTROL BITS OR SIGNALS (1)	
			P3DIR.x	P3SEL.x
P3.7/UCA1RXD/ UCA1SOMI	7	P3.7 (I/O)	0 = Input 1 = Output	0
		UCA1RXD/UCA1SOMI (2)	X	1

6.10.5 Port P4 (P4.0 to P4.7), Input/Output With Schmitt Trigger

Figure 6-10 shows the port diagram. Table 6-19 summarizes the selection of the pin function.

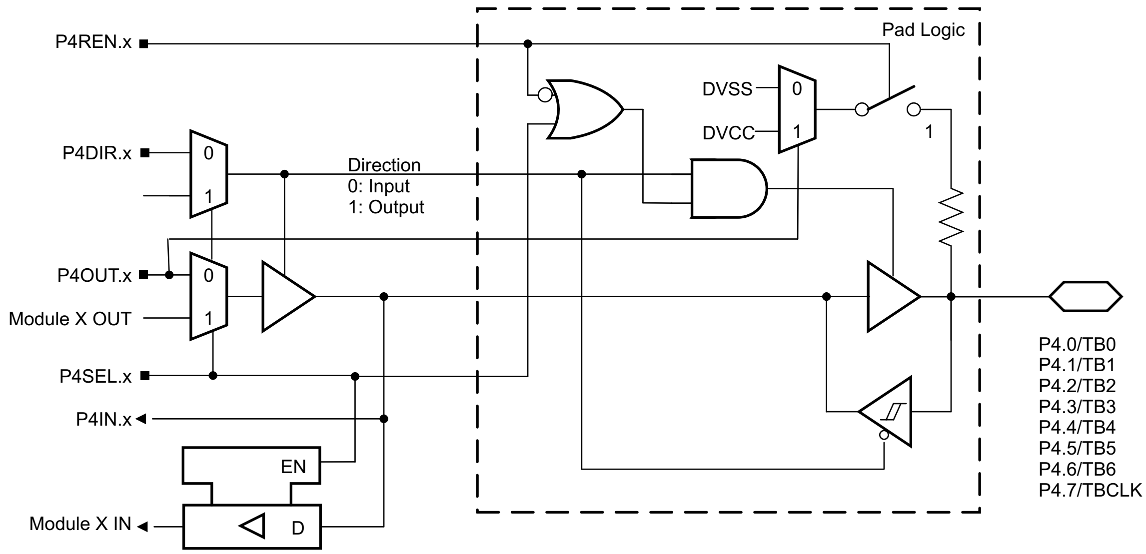


Figure 6-10. Port P4 (P4.0 to P4.7) Diagram

Table 6-19. Port P4 (P4.0 to P4.7) Pin Functions

PIN NAME (P4.x)	x	FUNCTION	CONTROL BITS OR SIGNALS (1)	
			P4DIR.x	P4SEL.x
P4.0/TB0	0	P4.0 (I/O)	0 = Input 1 = Output	0
		Timer_B7.CCI0A and Timer_B7.CCI0B	0	1
		Timer_B7.TB0	1	1
P4.1/TB1	1	P4.1 (I/O)	0 = Input 1 = Output	0
		Timer_B7.CCI1A and Timer_B7.CCI1B	0	1
		Timer_B7.TB1	1	1
P4.2/TB2	2	P4.2 (I/O)	0 = Input 1 = Output	0
		Timer_B7.CCI2A and Timer_B7.CCI2B	0	1
		Timer_B7.TB2	1	1
P4.3/TB3	3	P4.3 (I/O)	0 = Input 1 = Output	0
		Timer_B7.CCI3A and Timer_B7.CCI3B	0	1
		Timer_B7.TB3	1	1

(1) X = Don't care

Table 6-19. Port P4 (P4.0 to P4.7) Pin Functions (continued)

PIN NAME (P4.x)	x	FUNCTION	CONTROL BITS OR SIGNALS(1)	
			P4DIR.x	P4SEL.x
P4.4/TB4	4	P4.4 (I/O)	0 = Input 1 = Output	0
		Timer_B7.CCI4A and Timer_B7.CCI4B	0	1
		Timer_B7.TB4	1	1
P4.5/TB5	5	P4.5 (I/O)	0 = Input 1 = Output	0
		Timer_B7.CCI5A and Timer_B7.CCI5B	0	1
		Timer_B7.TB5	1	1
P4.6/TB6	6	P4.6 (I/O)	0 = Input 1 = Output	0
		Timer_B7.CCI6A and Timer_B7.CCI6B	0	1
		Timer_B7.TB6	1	1
P4.7/TBCLK	7	P4.7 (I/O)	0 = Input 1 = Output	0
		Timer_B7.TBCLK	0	1

6.10.6 Port P5 (P5.0 to P5.7), Input/Output With Schmitt Trigger

Figure 6-11 shows the port diagram. Table 6-20 summarizes the selection of the pin function.

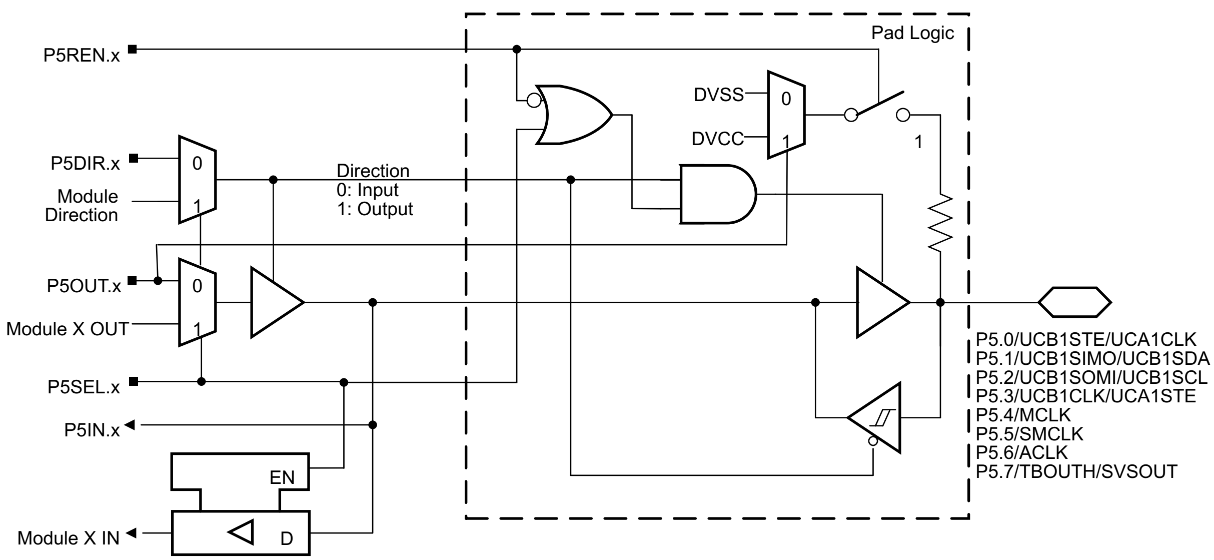


Figure 6-11. Port P5 (P5.0 to P5.7) Diagram

Table 6-20. Port P5 (P5.0 to P5.7) Pin Functions

PIN NAME (P5.x)	x	FUNCTION	CONTROL BITS OR SIGNALS(1)	
			P5DIR.x	P5SEL.x
P5.0/UCB1STE/ UCA1CLK	0	P5.0 (I/O)	0 = Input 1 = Output	0
		UCB1STE/UCA1CLK(2)(3)	X	1

(1) X = Don't care
(2) The pin direction is controlled by the USCI module.
(3) UCA1CLK function takes precedence over UCB1STE function. If the pin is required as UCA1CLK input or output, USCI_B1 is forced to 3-wire SPI mode if 4-wire SPI mode is selected.

Table 6-20. Port P5 (P5.0 to P5.7) Pin Functions (continued)

PIN NAME (P5.x)	x	FUNCTION	CONTROL BITS OR SIGNALS(1)	
			P5DIR.x	P5SEL.x
P5.1/UCB1SIMO/ UCB1SDA	1	P5.1 (I/O)	0 = Input 1 = Output	0
		UCB1SIMO/UCB1SDA(2)(4)	X	1
P5.2/UCB1SOMI/ UCB1SCL	2	P5.2 (I/O)	0 = Input 1 = Output	0
		UCB1SOMI/UCB1SCL(2)(4)	X	1
P5.3/UCB1CLK/ UCA1STE	3	P5.3 (I/O)	0 = Input 1 = Output	0
		UCB1CLK/UCA1STE(2)	X	1
P5.4/MCLK	4	P5.0 (I/O)	0 = Input 1 = Output	0
		MCLK	1	1
P5.5/SMCLK	5	P5.1 (I/O)	0 = Input 1 = Output	0
		SMCLK	1	1
P5.6/ACLK	6	P5.2 (I/O)	0 = Input 1 = Output	0
		ACLK	1	1
P5.7/TBOUTH/SVSOUT	7	P5.7 (I/O)	0 = Input 1 = Output	0
		TBOUTH	0	1
		SVSOUT	1	1

(4) If the I^2C functionality is selected, the output drives only the logical 0 to V_{SS} level.

6.10.7 Port P6 (P6.0 to P6.4), Input/Output With Schmitt Trigger

Figure 6-12 shows the port diagram. Table 6-21 summarizes the selection of the pin function.

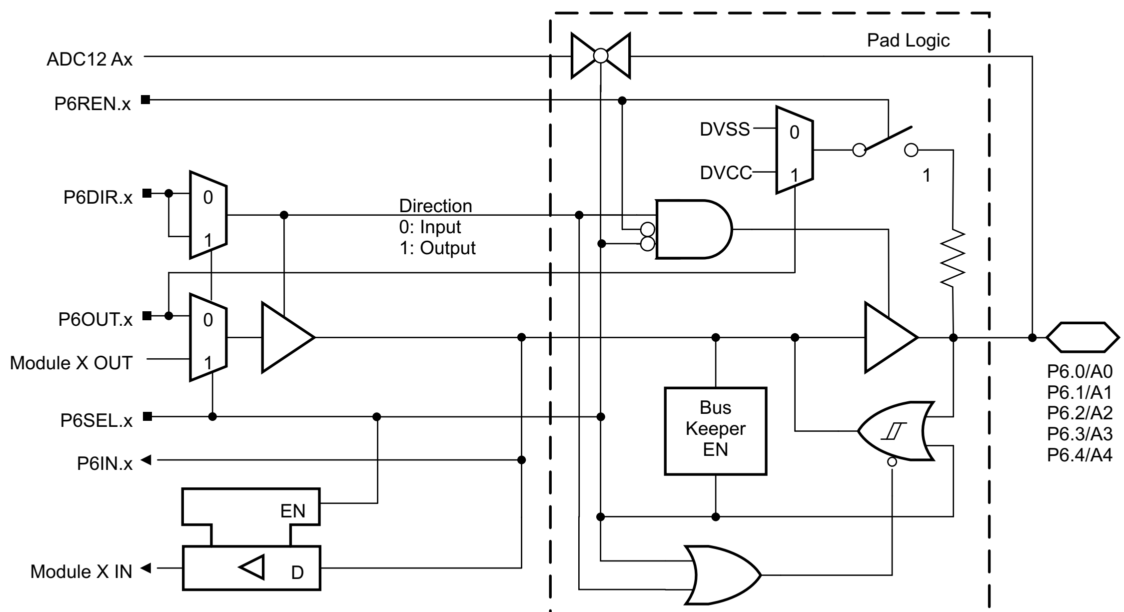


Figure 6-12. Port P6 (P6.0 to P6.4) Diagram

Table 6-21. Port P6 (P6.0 to P6.4) Pin Functions

PIN NAME (P6.x)	x	FUNCTION	CONTROL BITS OR SIGNALS(1)		
			P6DIR.x	P6SEL.x	INCH.x
P6.0/A0	0	P6.0 (I/O)	0 = Input 1 = Output	0	0
		A0(2)	X	1	1 (y = 0)
P6.1/A1	1	P6.1 (I/O)	0 = Input 1 = Output	0	0
		A1(2)	X	1	1 (y = 1)
P6.2/A2	2	P6.2 (I/O)	0 = Input 1 = Output	0	0
		A2(2)	X	1	1 (y = 2)
P6.3/A3	3	P6.3 (I/O)	0 = Input 1 = Output	0	0
		A3(2)	X	1	1 (y = 3)
P6.4/A4	4	P6.4 (I/O)	0 = Input 1 = Output	0	0
		A4(2)	X	1	1 (y = 4)

(1) X = Don't care
(2) The ADC12 channel Ax is connected to AV_{SS} internally if not selected.

6.10.8 Port P6 (P6.5 and P6.6), Input/Output With Schmitt Trigger

Figure 6-13 shows the port diagram. Table 6-22 summarizes the selection of the pin function.

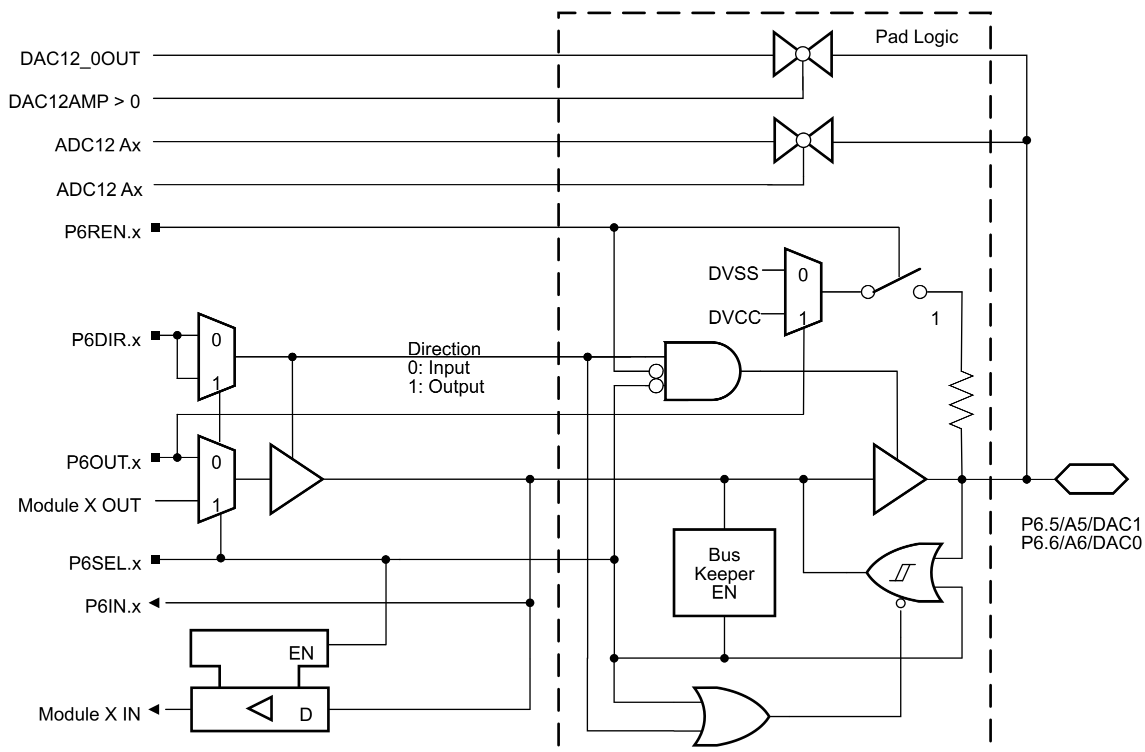


Figure 6-13. Port P6 (P6.5 and P6.6) Diagram

Table 6-22. Port P6 (P6.5 and P6.6) Pin Functions

PIN NAME (P6.x)	x	FUNCTION	CONTROL BITS OR SIGNALS (1)			
			P6DIR.x	P6SEL.x	DAC12AMP > 0	INCH.y
P6.5/A5/DAC1 (2)	5	P6.5 (I/O)	0 = Input 1 = Output	0	0	0
		DV_{SS}	1	1	0	0
		A5 (3)	X	X	0	1 (y = 5)
		DAC1 (DAC12OPS = 1) (4)	X	X	1	0
P6.6/A6/DAC0 (2)	6	P6.6 (I/O)	0 = Input 1 = Output	0	0	0
		DV_{SS}	1	1	0	0
		A6 (3)	X	X	0	1 (y = 6)
		DAC0 (DAC12OPS = 0) (4)	X	X	1	0

(1) X = Don't care
(2) MSP430F261x devices only
(3) The ADC12 channel Ax is connected to AV_{SS} internally if not selected.
(4) The DAC outputs are floating if not selected.

6.10.9 Port P6 (P6.7), Input/Output With Schmitt Trigger

Figure 6-14 shows the port diagram. Table 6-23 summarizes the selection of the pin function.

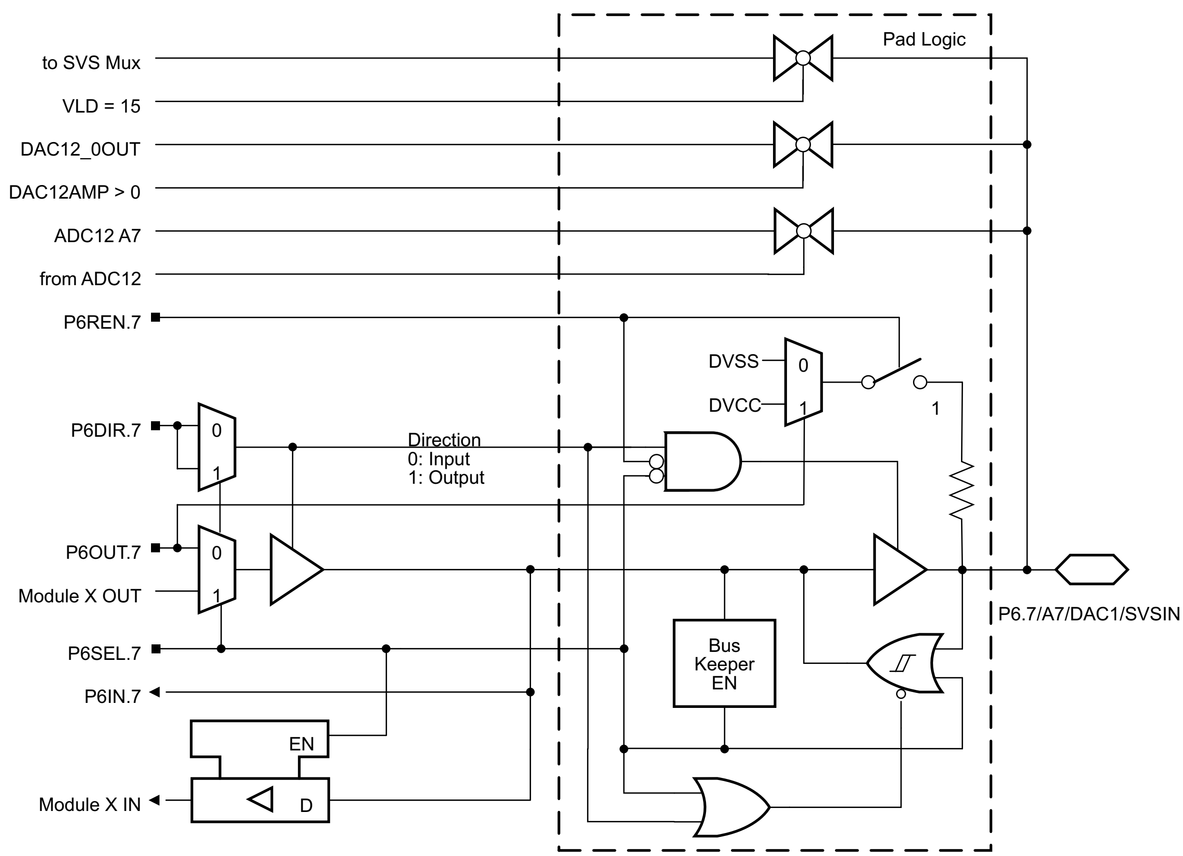


Figure 6-14. Port P6 (P6.7) Diagram

Table 6-23. Port P6 (P6.7) Pin Functions

PIN NAME (P6.x)	x	FUNCTION	CONTROL BITS OR SIGNALS(1)			
			P6DIR.x	P6SEL.x	INCH.y	DAC12AMP>0
P6.7/A7/DAC1(2)/ SVSIN(2)	7	P6.7 (I/O)	0 = Input 1 = Output	0	0	0
		DV_{SS}	1	1	0	0
		A7(3)	X	1	1 (y = 7)	0
		DAC1 (DAC12OPS = 0)(4)	X	1	0	1
		SVSIN (VLD = 15)	X	1	0	0

(1) X = Don't care
(2) MSP430F261x devices only
(3) The ADC12 channel Ax is connected to AV_{SS} internally if not selected.
(4) The DAC outputs are floating if not selected.

6.10.10 Port P7 (P7.0 to P7.7), Input/Output With Schmitt Trigger

Port P7 is available on 80-pin PN and 113-pin ZCA or ZQW devices only.

Figure 6-15 shows the port diagram. Table 6-24 summarizes the selection of the pin function.

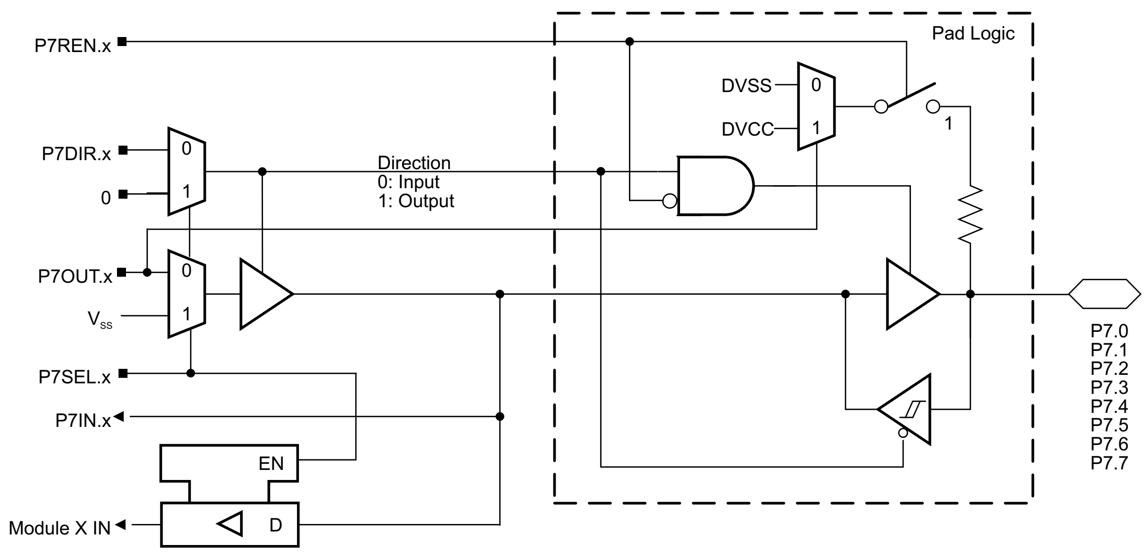


Figure 6-15. Port P7 (P7.0 to P7.7) Diagram

Table 6-24. Port P7 (P7.0 to P7.7) Pin Functions

PIN NAME (P7.x)	x	FUNCTION	CONTROL BITS OR SIGNALS(1)	
			P7DIR.x	P7SEL.x
P7.0	0	P7.0 (I/O)	0 = Input 1 = Output	0
		Input	X	1
P7.1	1	P7.1 (I/O)	0 = Input 1 = Output	0
		Input	X	1
P7.2	2	P7.2 (I/O)	0 = Input 1 = Output	0
		Input	X	1
P7.3	3	P7.3 (I/O)	0 = Input 1 = Output	0
		Input	X	1

(1) X = Don't care

Table 6-24. Port P7 (P7.0 to P7.7) Pin Functions (continued)

PIN NAME (P7.x)	x	FUNCTION	CONTROL BITS OR SIGNALS[(1)]	
			P7DIR.x	P7SEL.x
P7.4	4	P7.4 (I/O)	0 = Input 1 = Output	0
		Input	X	1
P7.5	5	P7.5 (I/O)	0 = Input 1 = Output	0
		Input	X	1
P7.6	6	P7.6 (I/O)	0 = Input 1 = Output	0
		Input	X	1
P7.7	7	P7.7 (I/O)	0 = Input 1 = Output	0
		Input	X	1

6.10.11 Port P8 (P8.0 to P8.5), Input/Output With Schmitt Trigger

Port P8 is available on 80-pin PN and 113-pin ZCA or ZQW devices only.

Figure 6-16 shows the port diagram. Table 6-25 summarizes the selection of the pin function.

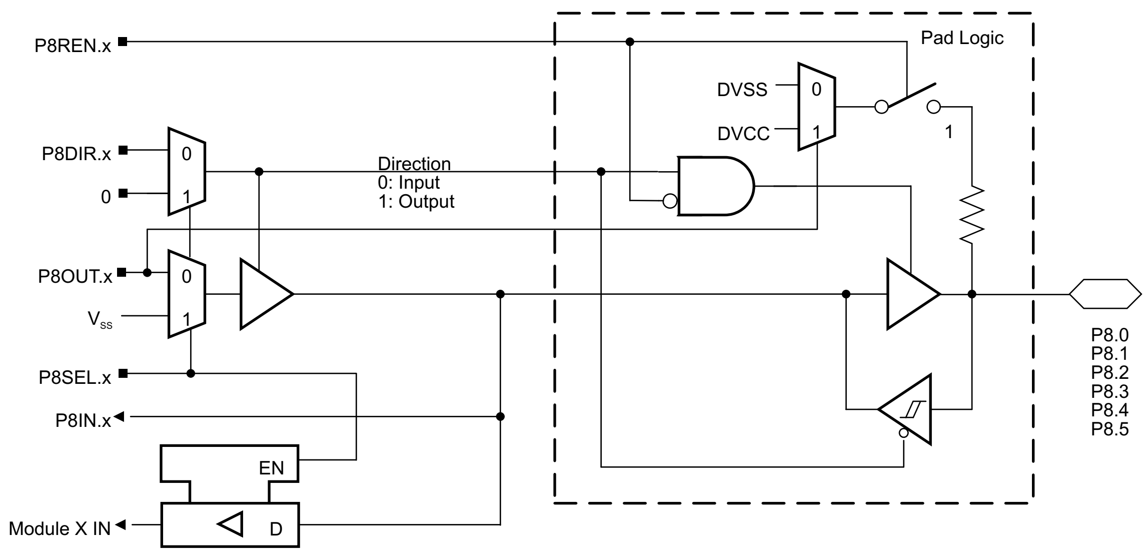


Figure 6-16. Port P8 (P8.0 to P8.5) Diagram

Table 6-25. Port P8 (P8.0 to P8.5) Pin Functions

PIN NAME (P8.x)	x	FUNCTION	CONTROL BITS OR SIGNALS[(1)]	
			P8DIR.x	P8SEL.x
P8.0	0	P8.0 (I/O)	0 = Input 1 = Output	0
		Input	X	1
P8.1	1	P8.1 (I/O)	0 = Input 1 = Output	0
		Input	X	1
P8.2	2	P8.2 (I/O)	0 = Input 1 = Output	0
		Input	X	1

(1) X = Don't care

Table 6-25. Port P8 (P8.0 to P8.5) Pin Functions (continued)

PIN NAME (P8.x)	x	FUNCTION	CONTROL BITS OR SIGNALS (1)	
			P8DIR.x	P8SEL.x
P8.3	3	P8.3 (I/O)	0 = Input 1 = Output	0
		Input	X	1
P8.4	4	P8.4 (I/O)	0 = Input 1 = Output	0
		Input	X	1
P8.5	5	P8.5 (I/O)	0 = Input 1 = Output	0
		Input	X	1

6.10.12 Port P8 (P8.6), Input/Output With Schmitt Trigger

Port P8 is available on 80-pin PN and 113-pin ZCA or ZQW devices only.

Figure 6-17 shows the port diagram. Table 6-26 summarizes the selection of the pin function.

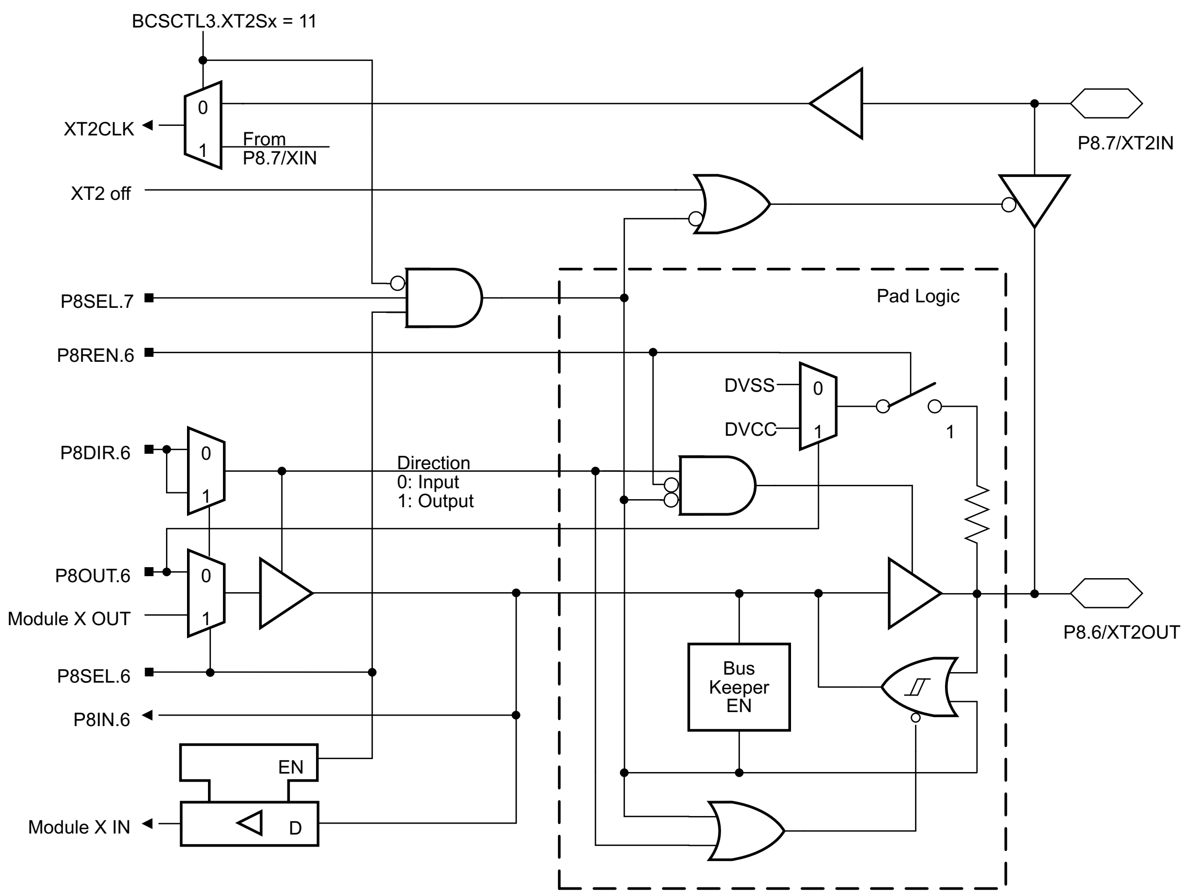


Figure 6-17. Port P8 (P8.6) Diagram

Table 6-26. Port P8 (P8.6) Pin Functions

PIN NAME (P8.x)	x	FUNCTION	CONTROL BITS OR SIGNALS	
			P8DIR.x	P8SEL.x
P8.6/XT2OUT	6	P8.6 (I/O)	0 = Input 1 = Output	0
		XT2OUT (default)	0	1
		DV_{SS}	1	1

6.10.13 Port P8 (P8.7), Input/Output With Schmitt Trigger

Port P8 is available on 80-pin PN and 113-pin ZCA or ZQW devices only.

Figure 6-18 shows the port diagram. Table 6-27 summarizes the selection of the pin function.

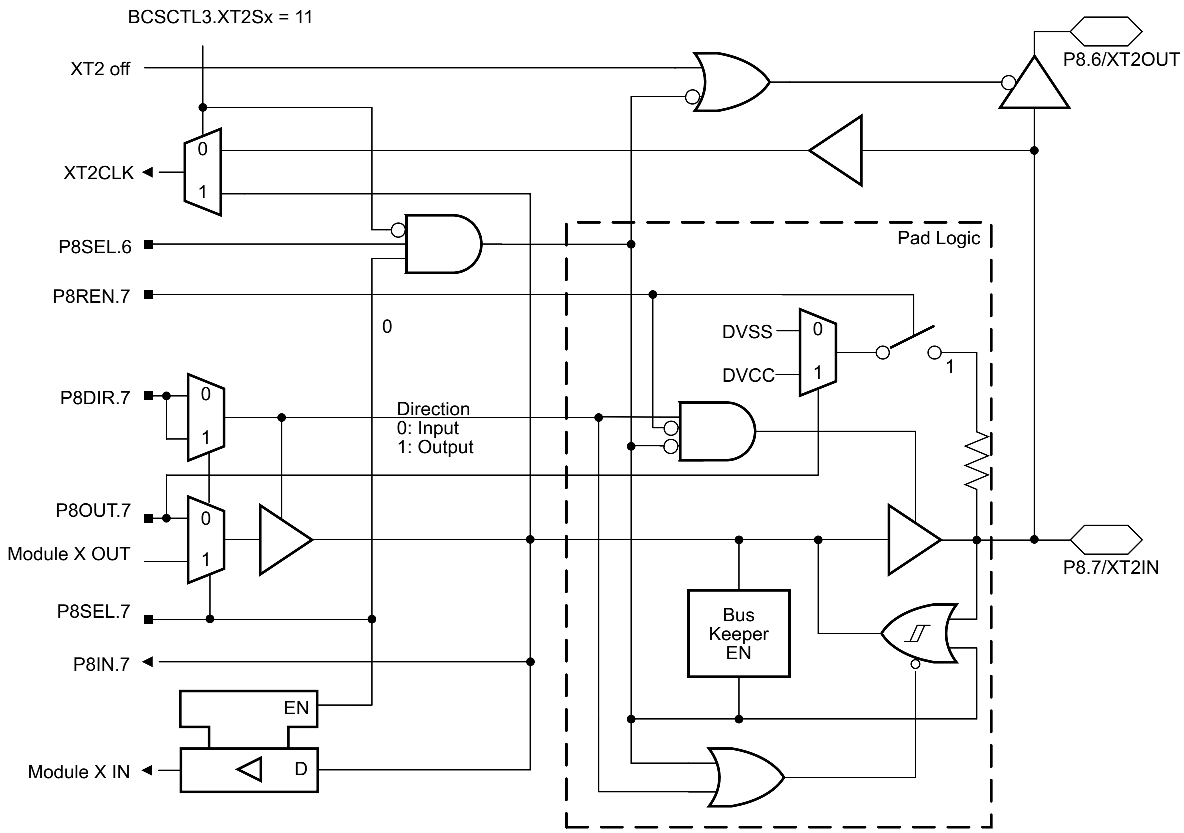


Figure 6-18. Port P8 (P8.7) Diagram

Table 6-27. Port P8 (P8.7) Pin Functions

PIN NAME (P8.x)	x	FUNCTION	CONTROL BITS OR SIGNALS	
			P8DIR.x	P8SEL.x
P8.7/XT2IN	7	P8.7 (I/O)	0 = Input 1 = Output	0
		XT2IN (default)	0	1
		V_{SS}	1	1

6.10.14 JTAG Pins (TMS, TCK, TDI/TCLK, TDO/TDI) Input/Output With Schmitt Trigger

Figure 6-19 shows the port diagram.

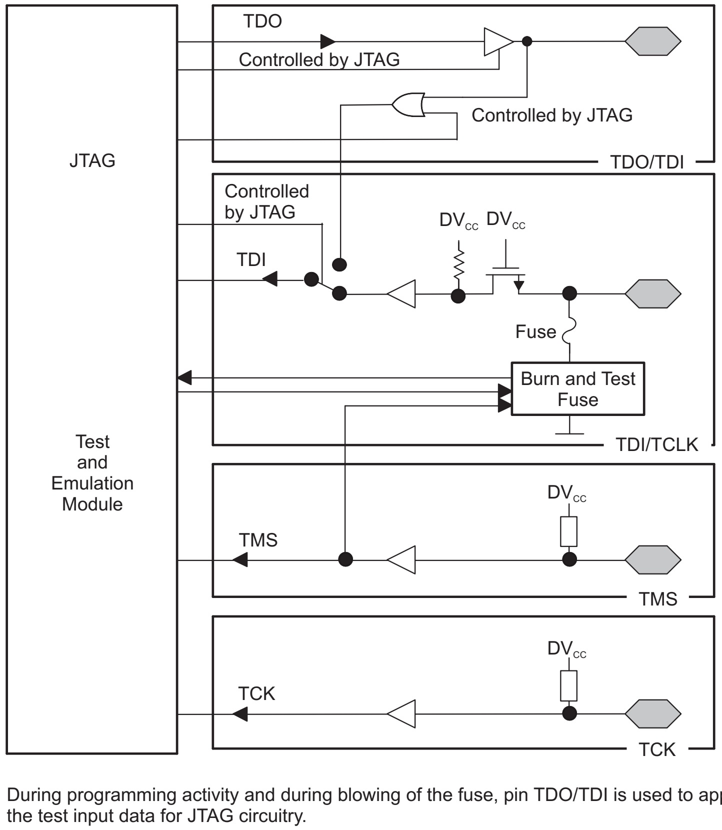


Figure 6-19. JTAG Pins (TMS, TCK, TDI/TCLK, TDO/TDI) Diagram

6.10.15 JTAG Fuse Check Mode

MSP430 devices that have the fuse on the TEST terminal have a fuse check mode that tests the continuity of the fuse the first time the JTAG port is accessed after a power-on reset (POR). When activated, a fuse check current (I_{TF}) of 1 mA at 3 V or 2.5 mA at 5 V can flow from the TEST pin to ground if the fuse is not burned. Take care to avoid accidentally activating the fuse check mode and increasing overall system power consumption.

When the TEST pin is again taken low after a test or programming session, the fuse check mode and sense currents are terminated.

Activation of the fuse check mode occurs with the first negative edge on the TMS pin after power up or if TMS is being held low during power up. The second positive edge on the TMS pin deactivates the fuse check mode. After deactivation, the fuse check mode remains inactive until another POR occurs. After each POR, the fuse check mode has the potential to be activated.

The fuse check current flows only when the fuse check mode is active and the TMS pin is in a low state (see Figure 6-20). Therefore, the additional current flow can be prevented by holding the TMS pin high (default condition).

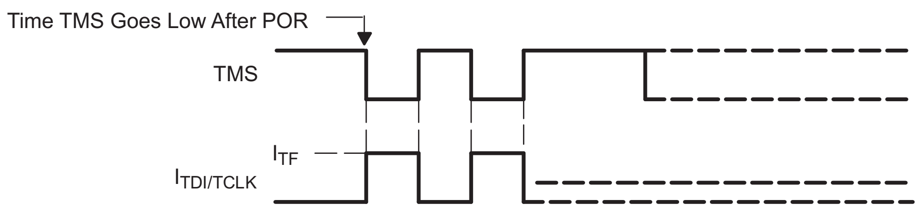


Figure 6-20. Fuse Check Mode Current

7 Device and Documentation Support

7.1 Getting Started

For more information on the MSP430 family of devices and the tools and libraries that are available to help with your development, visit the MSP430™ ultra-low-power sensing & measurement MCUs overview.

7.2 Device Nomenclature

To designate the stages in the product development cycle, TI assigns prefixes to the part numbers of all MSP MCU devices. Each MSP MCU commercial family member has one of two prefixes: MSP or XMS. These prefixes represent evolutionary stages of product development from engineering prototypes (XMS) through fully qualified production devices (MSP).

XMS – Experimental device that is not necessarily representative of the final device's electrical specifications

MSP – Fully qualified production device

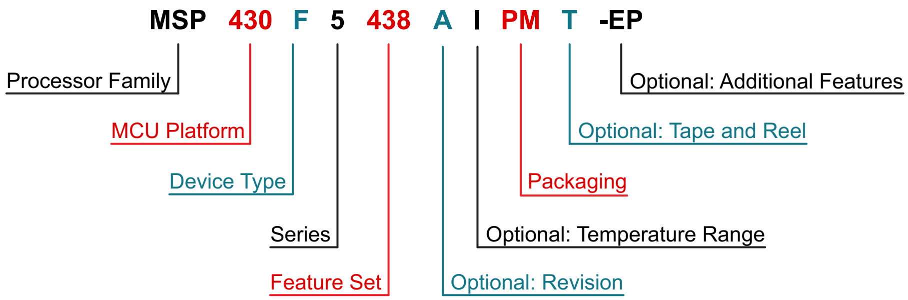
XMS devices are shipped against the following disclaimer:

"Developmental product is intended for internal evaluation purposes."

MSP devices have been characterized fully, and the quality and reliability of the device have been demonstrated fully. TI's standard warranty applies.

Predictions show that prototype devices (XMS) have a greater failure rate than the standard production devices. TI recommends that these devices not be used in any production system because their expected end-use failure rate still is undefined. Only qualified production devices are to be used.

TI device nomenclature also includes a suffix with the device family name. This suffix indicates the temperature range, package type, and distribution format. Figure 7-1 provides a legend for reading the complete device name.



Processor Family	CC = Embedded RF Radio MSP = Mixed-Signal Processor XMS = Experimental Silicon PMS = Prototype Device	
MCU Platform	430 = MSP430 low-power microcontroller platform	
Device Type	**Memory Type** C = ROM F = Flash FR = FRAM G = Flash L = No nonvolatile memory	**Specialized Application** AFE = Analog front end BQ = Contactless power CG = ROM medical FE = Flash energy meter FG = Flash medical FW = Flash electronic flow meter
Series	1 = Up to 8 MHz 2 = Up to 16 MHz 3 = Legacy 4 = Up to 16 MHz with LCD driver	5 = Up to 25 MHz 6 = Up to 25 MHz with LCD driver 0 = Low-voltage series
Feature Set	Various levels of integration within a series	
Optional: Revision	Updated version of the base part number	
Optional: Temperature Range	S = 0°C to 50°C C = 0°C to 70°C I = –40°C to 85°C T = –40°C to 105°C	
Packaging	http://www.ti.com/packaging	
Optional: Tape and Reel	T = Small reel R = Large reel No markings = Tube or tray	
Optional: Additional Features	-EP = Enhanced product (–40°C to 105°C) -HT = Extreme temperature parts (–55°C to 150°C) -Q1 = Automotive Q100 qualified	

Figure 7-1. Device Nomenclature

7.3 Tools and Software

Table 7-1 lists the debug features supported by the MSP430F261x and MSP430F241x microcontrollers. See the *Code Composer Studio IDE for MSP430 MCUs User's Guide* for details on the available features.

Table 7-1. Hardware Features

MSP430 ARCHITECTURE	4-WIRE JTAG	2-WIRE JTAG	BREAK-POINTS (N)	RANGE BREAK-POINTS	CLOCK CONTROL	STATE SEQUENCER	TRACE BUFFER
MSP430X	Yes	No	8	Yes	Yes	Yes	Yes

Design Kits and Evaluation Modules

64-pin Target Development Board and MSP-FET Programmer Bundle - MSP430F1x, MSP430F2x, MSP430F4x MCUs

The MSP-FET430U64 is a powerful flash emulation tool that includes the hardware and software required to quickly begin application development on the MSP430 MCU. It includes a ZIF socket target board (MSP-TS430PM64) and a USB debugging interface (MSP-FET) used to program and debug the MSP430 in-system through the JTAG interface or the pin-saving Spy-Bi-Wire (2-wire JTAG) protocol. The flash memory can be erased and programmed in seconds with only a few keystrokes, and because the MSP430 flash is ultra-low power, no external power supply is required.

80-pin Target Development Board and MSP-FET Programmer Bundle for MSP430F2x and MSP430F4x MCUs

The MSP-FET430U80 is a powerful flash emulation tool that includes the hardware and software required to quickly begin application development on the MSP430 MCU. It includes a ZIF socket target board and a USB debugging interface (MSP-FET) used to program and debug the MSP430 in-system through the JTAG interface or the pin-saving Spy-Bi-Wire (2-wire JTAG) protocol. The flash memory can be erased and programmed in seconds with only a few keystrokes, and because the MSP430 flash is ultra-low power, no external power supply is required.

Software

MSP430F241x, MSP430F261x Code Examples

C code examples are available for every MSP device that configures each of the integrated peripherals for various application needs.

MSPWare Software

MSPWare software is a collection of code examples, data sheets, and other design resources for all MSP devices delivered in a convenient package. In addition to providing a complete collection of existing MSP design resources, MSPWare software also includes a high-level API called MSP Driver Library. This library makes it easy to program MSP hardware. MSPWare software is available as a component of CCS or as a stand-alone package.

MSP Driver Library

The abstracted API of MSP Driver Library provides easy-to-use function calls that free you from directly manipulating the bits and bytes of the MSP430 hardware. Thorough documentation is delivered through a helpful API Guide, which includes details on each function call and the recognized parameters. Developers can use Driver Library functions to write complete projects with minimal overhead.

MSP EnergyTrace Technology

EnergyTrace technology for MSP430 microcontrollers is an energy-based code analysis tool that measures and displays the energy profile of the application and helps to optimize it for ultra-low power consumption.

ULP (Ultra-Low Power) Advisor

ULP Advisor™ software is a tool for guiding developers to write more efficient code to fully use the unique ultra-low-power features of MSP and MSP432 microcontrollers. Aimed at both experienced and new microcontroller developers, ULP Advisor checks your code against a thorough ULP checklist to help minimize the energy consumption of your application. At build time, ULP Advisor provides notifications and remarks to highlight areas of your code that can be further optimized for lower power.

Fixed Point Math Library for MSP

The MSP IQmath and Qmath Libraries are a collection of highly optimized and high-precision mathematical functions for C programmers to seamlessly port a floating-point algorithm into fixed-point code on MSP430 and MSP432 devices. These routines are typically used in computationally intensive real-time applications where optimal execution speed, high accuracy, and ultra-low energy are critical. By using the IQmath and Qmath libraries, it is possible to achieve execution speeds considerably faster and energy consumption considerably lower than equivalent code written using floating-point math.

Development Tools

Code Composer Studio™ Integrated Development Environment for MSP Microcontrollers

Code Composer Studio (CCS) integrated development environment (IDE) supports all MSP microcontroller devices. CCS comprises a suite of embedded software utilities used to develop and debug embedded applications. CCS includes an optimizing C/C++ compiler, source code editor, project build environment, debugger, profiler, and many other features.

MSPWare Software

MSPWare software is a collection of code examples, data sheets, and other design resources for all MSP devices delivered in a convenient package. In addition to providing a complete collection of existing MSP design resources, MSPWare software also includes a high-level API called MSP Driver Library. This library makes it easy to program MSP hardware. MSPWare software is available as a component of CCS or as a stand-alone package.

Command-Line Programmer

MSP Flasher is an open-source shell-based interface for programming MSP microcontrollers through a FET programmer or eZ430 using JTAG or Spy-Bi-Wire (SBW) communication. MSP Flasher can download binary files (.txt or .hex) directly to the MSP microcontroller without an IDE.

MSP MCU Programmer and Debugger

The MSP-FET is a powerful emulation development tool – often called a debug probe – which lets users quickly begin application development on MSP low-power MCUs. Creating MCU software usually requires downloading the resulting binary program to the MSP device for validation and debugging.

MSP-GANG Production Programmer

The MSP Gang Programmer is an MSP430 or MSP432 device programmer that can program up to eight identical MSP430 or MSP432 flash or FRAM devices at the same time. The MSP Gang Programmer connects to a host PC using a standard RS-232 or USB connection and provides flexible programming options that let the user fully customize the process.

7.4 Documentation Support

The following documents describe the MSP430F261x and MSP430F241x MCUs. Copies of these documents are available on the Internet at www.ti.com.

Receiving Notification of Document Updates

To receive notification of documentation updates—including silicon errata—go to the product folder for your device on ti.com (see Section 7.5 for links to product folders). In the upper right corner, click the "Alert me" button. This registers you to receive a weekly digest of product information that has changed (if any). For change details, check the revision history of any revised document.

Errata

MSP430F2619 Device Erratasheet

Describes the known exceptions to the functional specifications.

MSP430F2618 Device Erratasheet

Describes the known exceptions to the functional specifications.

MSP430F2617 Device Erratasheet

Describes the known exceptions to the functional specifications.

MSP430F2616 Device Erratasheet

Describes the known exceptions to the functional specifications.

MSP430F2419 Device Erratasheet

Describes the known exceptions to the functional specifications.

MSP430F2418 Device Erratasheet

Describes the known exceptions to the functional specifications.

MSP430F2417 Device Erratasheet

Describes the known exceptions to the functional specifications.

MSP430F2416 Device Erratasheet

Describes the known exceptions to the functional specifications.

User's Guides

MSP430F2xx, MSP430G2xx Family User's Guide

Detailed description of all modules and peripherals available in this device family.

MSP430 Programming With the JTAG Interface

This document describes the functions that are required to erase, program, and verify the memory module of the MSP430 flash-based and FRAM-based microcontroller families using the JTAG communication port. In addition, it describes how to program the JTAG access security fuse that is available on all MSP430 devices. This document describes device access using both the standard 4-wire JTAG interface and the 2-wire JTAG interface, which is also referred to as Spy-Bi-Wire (SBW).

MSP430 Flash Device Bootloader (BSL) User's Guide

The MSP430 BSL lets users communicate with embedded memory in the MSP430 MCU during the prototyping phase, final production, and in service. Both the programmable memory (flash memory) and the data memory (RAM) can be modified as required.

MSP430 Hardware Tools User's Guide

This manual describes the hardware of the TI MSP-FET430 Flash Emulation Tool (FET). The FET is the program development tool for the MSP430 ultra-low-power microcontroller. Both available interface types, the parallel port interface and the USB interface, are described.

Application Reports

MSP430 32-kHz Crystal Oscillators

Selection of the right crystal, correct load circuit, and proper board layout are important for a stable crystal oscillator. This application report summarizes crystal oscillator function and explains the parameters to select the correct crystal for MSP430 ultra-low-power operation. In addition, hints and examples for correct board layout are given. The document also contains detailed information on the possible oscillator tests to ensure stable oscillator operation in mass production.

MSP430 System-Level ESD Considerations

System-level ESD has become increasingly demanding with silicon technology scaling towards lower voltages and the need for designing cost-effective and ultra-low-power components. This application report addresses three different ESD topics to help board designers and OEMs understand and design robust system-level designs.

Understanding MSP430 Flash Data Retention

The MSP430 family of microcontrollers, as part of its broad portfolio, offers both read-only memory (ROM)-based and flash-based devices. Understanding the MSP430 flash is extremely important for efficient, robust, and reliable system design. Data retention is one of the key aspects to flash reliability. In this application report, data retention for the MSP430 flash is discussed in detail and the effect of temperature is given primary importance.

Interfacing the 3-V MSP430 to 5-V Circuits

The interfacing of the 3-V MSP430x1xx and MSP430x4xx microcontroller families to circuits with a supply of 5 V or higher is shown. Input, output and I/O interfaces are given and explained. Worse-case design equations are provided, where necessary. Some simple power supplies generating both voltages are shown, too.

Efficient Multiplication and Division Using MSP430

Multiplication and division in the absence of a hardware multiplier require many instruction cycles, especially in C. This report discusses a method that does not need a hardware multiplier and can perform multiplication and division with only shift and add instructions. The method described in this application report is based on Horner's method.

7.5 Related Links

Table 7-2 lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 7-2. Related Links

PARTS	PRODUCT FOLDER	ORDER NOW	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
MSP430F2619	Click here	Click here	Click here	Click here	Click here
MSP430F2618	Click here	Click here	Click here	Click here	Click here
MSP430F2617	Click here	Click here	Click here	Click here	Click here
MSP430F2616	Click here	Click here	Click here	Click here	Click here
MSP430F2419	Click here	Click here	Click here	Click here	Click here
MSP430F2418	Click here	Click here	Click here	Click here	Click here
MSP430F2417	Click here	Click here	Click here	Click here	Click here
MSP430F2416	Click here	Click here	Click here	Click here	Click here

7.6 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Community
TI's Engineer-to-Engineer (E2E) Community. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas, and help solve problems with fellow engineers.

TI Embedded Processors Wiki
Texas Instruments Embedded Processors Wiki. Established to help developers get started with embedded processors from Texas Instruments and to foster innovation and growth of general knowledge about the hardware and software surrounding these devices.

7.7 Trademarks

MSP430, MicroStar Junior, ULP Advisor, Code Composer Studio, E2E are trademarks of Texas Instruments.

7.8 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

7.9 Export Control Notice

Recipient agrees to not knowingly export or re-export, directly or indirectly, any product or technical data (as defined by the U.S., EU, and other Export Administration Regulations) including software, or any controlled product restricted by other applicable national regulations, received from disclosing party under nondisclosure obligations (if any), or any direct product of such technology, to any destination to which such export or re-export is restricted or prohibited by U.S. or other applicable laws, without obtaining prior authorization from U.S. Department of Commerce and other competent Government authorities to the extent required by those laws.

7.10 Glossary

TI Glossary This glossary lists and explains terms, acronyms, and definitions.

8 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
MSP430F2416TPM	ACTIVE	LQFP	PM	64	160	Green (RoHS & no Sb/Br)	NIPDAU	Level-3-260C-168 HR	-40 to 105	M430F2416T	Samples
MSP430F2416TPMR	ACTIVE	LQFP	PM	64	1000	Green (RoHS & no Sb/Br)	NIPDAU	Level-3-260C-168 HR	-40 to 105	M430F2416T	Samples
MSP430F2416TPN	ACTIVE	LQFP	PN	80	119	Green (RoHS & no Sb/Br)	NIPDAU	Level-3-260C-168 HR	-40 to 105	M430F2416T	Samples
MSP430F2416TPNR	ACTIVE	LQFP	PN	80	1000	Green (RoHS & no Sb/Br)	NIPDAU	Level-3-260C-168 HR	-40 to 105	M430F2416T	Samples
MSP430F2416TZCA	ACTIVE	NFBGA	ZCA	113	260	Green (RoHS & no Sb/Br)	SNAGCU	Level-3-260C-168 HR	-40 to 105	F2416T	Samples
MSP430F2416TZCAR	ACTIVE	NFBGA	ZCA	113	2500	Green (RoHS & no Sb/Br)	SNAGCU	Level-3-260C-168 HR	-40 to 105	F2416T	Samples
MSP430F2416TZQW	LIFEBUY	BGA MICROSTAR JUNIOR	ZQW	113	260	Green (RoHS & no Sb/Br)	SNAGCU	Level-3-260C-168 HR	0 to 0	M430F2416T	
MSP430F2416TZQWR	LIFEBUY	BGA MICROSTAR JUNIOR	ZQW	113	2500	Green (RoHS & no Sb/Br)	SNAGCU	Level-3-260C-168 HR	0 to 0	M430F2416T	
MSP430F2417TPM	ACTIVE	LQFP	PM	64	160	Green (RoHS & no Sb/Br)	NIPDAU	Level-3-260C-168 HR	-40 to 105	M430F2417T	Samples
MSP430F2417TPMR	ACTIVE	LQFP	PM	64	1000	Green (RoHS & no Sb/Br)	NIPDAU	Level-3-260C-168 HR	-40 to 105	M430F2417T	Samples
MSP430F2417TPN	ACTIVE	LQFP	PN	80	119	Green (RoHS & no Sb/Br)	NIPDAU	Level-3-260C-168 HR	-40 to 105	M430F2417T	Samples
MSP430F2417TPNR	ACTIVE	LQFP	PN	80	1000	Green (RoHS & no Sb/Br)	NIPDAU	Level-3-260C-168 HR	-40 to 105	M430F2417T	Samples
MSP430F2417TZCAR	ACTIVE	NFBGA	ZCA	113	2500	Green (RoHS & no Sb/Br)	SNAGCU	Level-3-260C-168 HR	-40 to 105	F2417T	Samples
MSP430F2417TZQWR	LIFEBUY	BGA MICROSTAR JUNIOR	ZQW	113	2500	Green (RoHS & no Sb/Br)	SNAGCU	Level-3-260C-168 HR	0 to 0	M430F2417T	
MSP430F2418TPM	ACTIVE	LQFP	PM	64	160	Green (RoHS & no Sb/Br)	NIPDAU	Level-3-260C-168 HR	-40 to 105	M430F2418T	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
MSP430F2418TPMR	ACTIVE	LQFP	PM	64	1000	Green (RoHS & no Sb/Br)	NIPDAU	Level-3-260C-168 HR	-40 to 105	M430F2418T	Samples
MSP430F2418TPN	ACTIVE	LQFP	PN	80	119	Green (RoHS & no Sb/Br)	NIPDAU	Level-3-260C-168 HR	-40 to 105	M430F2418T	Samples
MSP430F2418TPNR	ACTIVE	LQFP	PN	80	1000	Green (RoHS & no Sb/Br)	NIPDAU	Level-3-260C-168 HR	-40 to 105	M430F2418T	Samples
MSP430F2418TZCA	ACTIVE	NFBGA	ZCA	113	260	Green (RoHS & no Sb/Br)	SNAGCU	Level-3-260C-168 HR	-40 to 105	F2418T	Samples
MSP430F2418TZCAR	ACTIVE	NFBGA	ZCA	113	2500	Green (RoHS & no Sb/Br)	SNAGCU	Level-3-260C-168 HR	-40 to 105	F2418T	Samples
MSP430F2418TZQW	LIFEBUY	BGA MICROSTAR JUNIOR	ZQW	113	260	Green (RoHS & no Sb/Br)	SNAGCU	Level-3-260C-168 HR	0 to 0	M430F2418T	
MSP430F2418TZQWR	LIFEBUY	BGA MICROSTAR JUNIOR	ZQW	113	2500	Green (RoHS & no Sb/Br)	SNAGCU	Level-3-260C-168 HR	0 to 0	M430F2418T	
MSP430F2419TPM	ACTIVE	LQFP	PM	64	160	Green (RoHS & no Sb/Br)	NIPDAU	Level-3-260C-168 HR	-40 to 105	M430F2419T	Samples
MSP430F2419TPMR	ACTIVE	LQFP	PM	64	1000	Green (RoHS & no Sb/Br)	NIPDAU	Level-3-260C-168 HR	-40 to 105	M430F2419T	Samples
MSP430F2419TPN	ACTIVE	LQFP	PN	80	119	Green (RoHS & no Sb/Br)	NIPDAU	Level-3-260C-168 HR	-40 to 105	M430F2419T	Samples
MSP430F2419TPNR	ACTIVE	LQFP	PN	80	1000	Green (RoHS & no Sb/Br)	NIPDAU	Level-3-260C-168 HR	-40 to 105	M430F2419T	Samples
MSP430F2419TZQW	LIFEBUY	BGA MICROSTAR JUNIOR	ZQW	113	260	Green (RoHS & no Sb/Br)	SNAGCU	Level-3-260C-168 HR	0 to 0	M430F2419T	
MSP430F2419TZQWR	LIFEBUY	BGA MICROSTAR JUNIOR	ZQW	113	2500	Green (RoHS & no Sb/Br)	SNAGCU	Level-3-260C-168 HR	0 to 0	M430F2419T	
MSP430F2616TPM	ACTIVE	LQFP	PM	64	160	Green (RoHS & no Sb/Br)	NIPDAU	Level-3-260C-168 HR	-40 to 105	M430F2616T	Samples
MSP430F2616TPMR	ACTIVE	LQFP	PM	64	1000	Green (RoHS & no Sb/Br)	NIPDAU	Level-3-260C-168 HR	-40 to 105	M430F2616T	Samples
MSP430F2616TPN	ACTIVE	LQFP	PN	80	119	Green (RoHS & no Sb/Br)	NIPDAU	Level-3-260C-168 HR	-40 to 105	M430F2616T	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
MSP430F2616TPNR	ACTIVE	LQFP	PN	80	1000	Green (RoHS & no Sb/Br)	NIPDAU	Level-3-260C-168 HR	-40 to 105	M430F2616T	Samples
MSP430F2616TZCA	ACTIVE	NFBGA	ZCA	113	260	Green (RoHS & no Sb/Br)	SNAGCU	Level-3-260C-168 HR	-40 to 105	F2616T	Samples
MSP430F2616TZCAR	ACTIVE	NFBGA	ZCA	113	2500	Green (RoHS & no Sb/Br)	SNAGCU	Level-3-260C-168 HR	-40 to 105	F2616T	Samples
MSP430F2616TZQW	LIFEBUY	BGA MICROSTAR JUNIOR	ZQW	113	260	Green (RoHS & no Sb/Br)	SNAGCU	Level-3-260C-168 HR	0 to 0	M430F2616T	
MSP430F2616TZQWR	LIFEBUY	BGA MICROSTAR JUNIOR	ZQW	113	2500	Green (RoHS & no Sb/Br)	SNAGCU	Level-3-260C-168 HR	0 to 0	M430F2616T	
MSP430F2617TPM	ACTIVE	LQFP	PM	64	160	Green (RoHS & no Sb/Br)	NIPDAU	Level-3-260C-168 HR	-40 to 105	M430F2617T	Samples
MSP430F2617TPMR	ACTIVE	LQFP	PM	64	1000	Green (RoHS & no Sb/Br)	NIPDAU	Level-3-260C-168 HR	-40 to 105	M430F2617T	Samples
MSP430F2617TPN	ACTIVE	LQFP	PN	80	119	Green (RoHS & no Sb/Br)	NIPDAU	Level-3-260C-168 HR	-40 to 105	M430F2617T	Samples
MSP430F2617TPNR	ACTIVE	LQFP	PN	80	1000	Green (RoHS & no Sb/Br)	NIPDAU	Level-3-260C-168 HR	-40 to 105	M430F2617T	Samples
MSP430F2617TZCA	ACTIVE	NFBGA	ZCA	113	260	Green (RoHS & no Sb/Br)	SNAGCU	Level-3-260C-168 HR	-40 to 105	F2617T	Samples
MSP430F2617TZCAR	ACTIVE	NFBGA	ZCA	113	2500	Green (RoHS & no Sb/Br)	SNAGCU	Level-3-260C-168 HR	-40 to 105	F2617T	Samples
MSP430F2617TZQW	LIFEBUY	BGA MICROSTAR JUNIOR	ZQW	113	260	Green (RoHS & no Sb/Br)	SNAGCU	Level-3-260C-168 HR	0 to 0	M430F2617T	
MSP430F2617TZQWR	LIFEBUY	BGA MICROSTAR JUNIOR	ZQW	113	2500	Green (RoHS & no Sb/Br)	SNAGCU	Level-3-260C-168 HR	0 to 0	M430F2617T	
MSP430F2618TPM	ACTIVE	LQFP	PM	64	160	Green (RoHS & no Sb/Br)	NIPDAU	Level-3-260C-168 HR	-40 to 105	M430F2618T	Samples
MSP430F2618TPMR	ACTIVE	LQFP	PM	64	1000	Green (RoHS & no Sb/Br)	NIPDAU	Level-3-260C-168 HR	-40 to 105	M430F2618T	Samples
MSP430F2618TPN	ACTIVE	LQFP	PN	80	119	Green (RoHS & no Sb/Br)	NIPDAU	Level-3-260C-168 HR	-40 to 105	M430F2618T	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
MSP430F2618TPNR	ACTIVE	LQFP	PN	80	1000	Green (RoHS & no Sb/Br)	NIPDAU	Level-3-260C-168 HR	-40 to 105	M430F2618T	Samples
MSP430F2618TZCA	ACTIVE	NFBGA	ZCA	113	260	Green (RoHS & no Sb/Br)	SNAGCU	Level-3-260C-168 HR	-40 to 105	F2618T	Samples
MSP430F2618TZCAR	ACTIVE	NFBGA	ZCA	113	2500	Green (RoHS & no Sb/Br)	SNAGCU	Level-3-260C-168 HR	-40 to 105	F2618T	Samples
MSP430F2618TZQW	LIFEBUY	BGA MICROSTAR JUNIOR	ZQW	113	260	Green (RoHS & no Sb/Br)	SNAGCU	Level-3-260C-168 HR	0 to 0	M430F2618T	
MSP430F2618TZQWR	LIFEBUY	BGA MICROSTAR JUNIOR	ZQW	113	2500	Green (RoHS & no Sb/Br)	SNAGCU	Level-3-260C-168 HR	0 to 0	M430F2618T	
MSP430F2619TPM	ACTIVE	LQFP	PM	64	160	Green (RoHS & no Sb/Br)	NIPDAU	Level-3-260C-168 HR	-40 to 105	M430F2619T REV #	Samples
MSP430F2619TPMR	ACTIVE	LQFP	PM	64	1000	Green (RoHS & no Sb/Br)	NIPDAU	Level-3-260C-168 HR	-40 to 105	M430F2619T REV #	Samples
MSP430F2619TPN	ACTIVE	LQFP	PN	80	119	Green (RoHS & no Sb/Br)	NIPDAU	Level-3-260C-168 HR	-40 to 105	M430F2619T	Samples
MSP430F2619TPNR	ACTIVE	LQFP	PN	80	1000	Green (RoHS & no Sb/Br)	NIPDAU	Level-3-260C-168 HR	-40 to 105	M430F2619T	Samples
MSP430F2619TZCA	ACTIVE	NFBGA	ZCA	113	260	Green (RoHS & no Sb/Br)	SNAGCU	Level-3-260C-168 HR	-40 to 105	F2619T	Samples
MSP430F2619TZCAR	ACTIVE	NFBGA	ZCA	113	2500	Green (RoHS & no Sb/Br)	SNAGCU	Level-3-260C-168 HR	-40 to 105	F2619T	Samples
MSP430F2619TZQW	LIFEBUY	BGA MICROSTAR JUNIOR	ZQW	113	260	Green (RoHS & no Sb/Br)	SNAGCU	Level-3-260C-168 HR	0 to 0	M430F2619T	
MSP430F2619TZQWR	LIFEBUY	BGA MICROSTAR JUNIOR	ZQW	113	2500	Green (RoHS & no Sb/Br)	SNAGCU	Level-3-260C-168 HR	0 to 0	M430F2619T	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

[3] MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

[4] There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

[5] Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

[6] Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF MSP430F2618 :

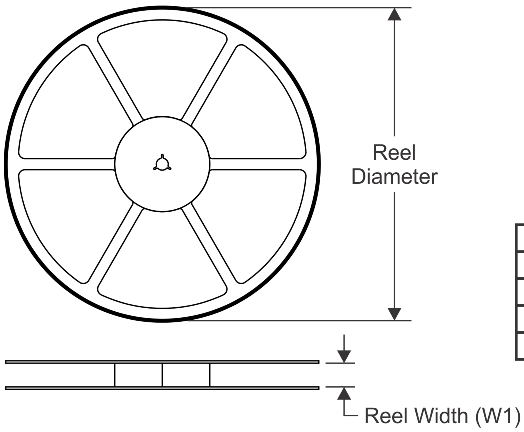
- Enhanced Product: MSP430F2618-EP

NOTE: Qualified Version Definitions:

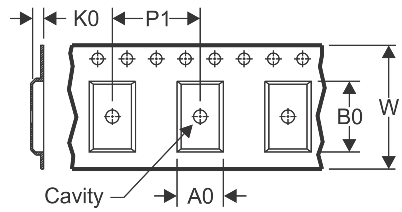
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

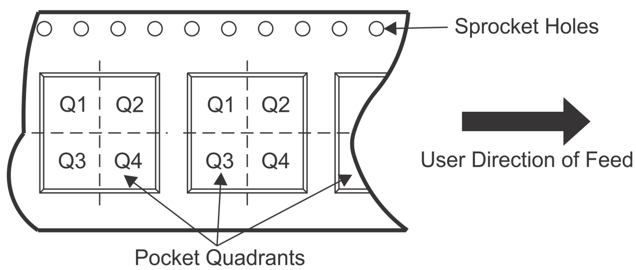


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

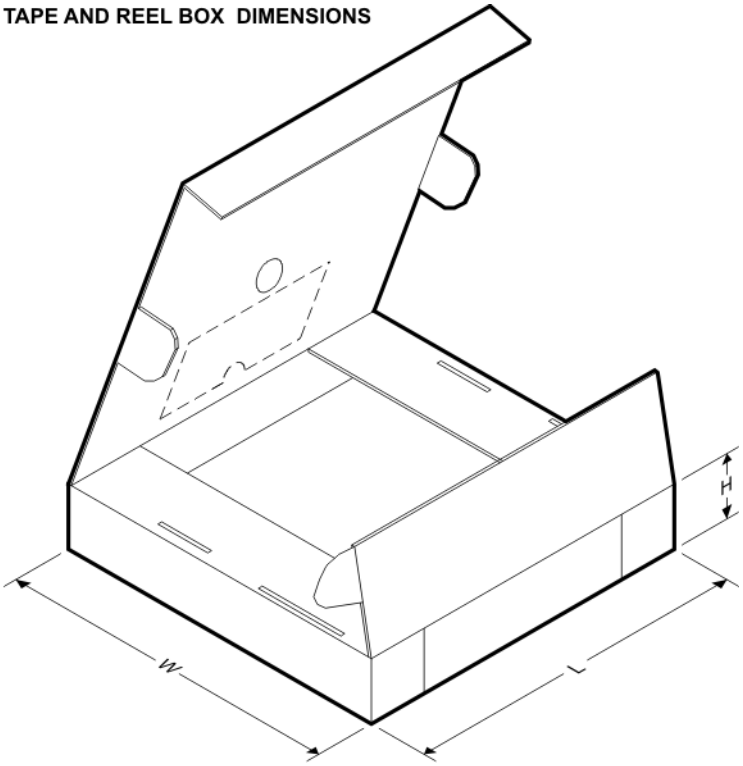


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
MSP430F2416TPMR	LQFP	PM	64	1000	330.0	24.4	13.0	13.0	2.1	16.0	24.0	Q2
MSP430F2416TPMR	LQFP	PM	64	1000	330.0	24.4	13.0	13.0	2.1	16.0	24.0	Q2
MSP430F2416TPNR	LQFP	PN	80	1000	330.0	24.4	15.0	15.0	2.1	20.0	24.0	Q2
MSP430F2416TZCAR	NFBGA	ZCA	113	2500	330.0	16.4	7.3	7.3	1.5	12.0	16.0	Q1
MSP430F2416TZQWR	BGA MI CROSTA R JUNI OR	ZQW	113	2500	330.0	16.4	7.3	7.3	1.5	12.0	16.0	Q1
MSP430F2417TPMR	LQFP	PM	64	1000	330.0	24.4	13.0	13.0	2.1	16.0	24.0	Q2
MSP430F2417TPMR	LQFP	PM	64	1000	330.0	24.4	13.0	13.0	2.1	16.0	24.0	Q2
MSP430F2417TPNR	LQFP	PN	80	1000	330.0	24.4	15.0	15.0	2.1	20.0	24.0	Q2
MSP430F2417TZCAR	NFBGA	ZCA	113	2500	330.0	16.4	7.3	7.3	1.5	12.0	16.0	Q1
MSP430F2417TZQWR	BGA MI CROSTA R JUNI OR	ZQW	113	2500	330.0	16.4	7.3	7.3	1.5	12.0	16.0	Q1
MSP430F2418TPMR	LQFP	PM	64	1000	330.0	24.4	13.0	13.0	2.1	16.0	24.0	Q2
MSP430F2418TPMR	LQFP	PM	64	1000	330.0	24.4	13.0	13.0	2.1	16.0	24.0	Q2
MSP430F2418TPNR	LQFP	PN	80	1000	330.0	24.4	15.0	15.0	2.1	20.0	24.0	Q2
MSP430F2418TZCAR	NFBGA	ZCA	113	2500	330.0	16.4	7.3	7.3	1.5	12.0	16.0	Q1

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
MSP430F2418TZQWR	BGA MICROSTAR JUNIOR	ZQW	113	2500	330.0	16.4	7.3	7.3	1.5	12.0	16.0	Q1
MSP430F2419TPMR	LQFP	PM	64	1000	330.0	24.4	13.0	13.0	2.1	16.0	24.0	Q2
MSP430F2419TPMR	LQFP	PM	64	1000	330.0	24.4	13.0	13.0	2.1	16.0	24.0	Q2
MSP430F2419TPNR	LQFP	PN	80	1000	330.0	24.4	15.0	15.0	2.1	20.0	24.0	Q2
MSP430F2419TZQWR	BGA MICROSTAR JUNIOR	ZQW	113	2500	330.0	16.4	7.3	7.3	1.5	12.0	16.0	Q1
MSP430F2616TPMR	LQFP	PM	64	1000	330.0	24.4	13.0	13.0	2.1	16.0	24.0	Q2
MSP430F2616TPMR	LQFP	PM	64	1000	330.0	24.4	13.0	13.0	2.1	16.0	24.0	Q2
MSP430F2616TPNR	LQFP	PN	80	1000	330.0	24.4	15.0	15.0	2.1	20.0	24.0	Q2
MSP430F2616TZCAR	NFBGA	ZCA	113	2500	330.0	16.4	7.3	7.3	1.5	12.0	16.0	Q1
MSP430F2616TZQWR	BGA MICROSTAR JUNIOR	ZQW	113	2500	330.0	16.4	7.3	7.3	1.5	12.0	16.0	Q1
MSP430F2617TPMR	LQFP	PM	64	1000	330.0	24.4	13.0	13.0	2.1	16.0	24.0	Q2
MSP430F2617TPMR	LQFP	PM	64	1000	330.0	24.4	13.0	13.0	2.1	16.0	24.0	Q2
MSP430F2617TPNR	LQFP	PN	80	1000	330.0	24.4	15.0	15.0	2.1	20.0	24.0	Q2
MSP430F2617TZCAR	NFBGA	ZCA	113	2500	330.0	16.4	7.3	7.3	1.5	12.0	16.0	Q1
MSP430F2617TZQWR	BGA MICROSTAR JUNIOR	ZQW	113	2500	330.0	16.4	7.3	7.3	1.5	12.0	16.0	Q1
MSP430F2618TPMR	LQFP	PM	64	1000	330.0	24.4	13.0	13.0	2.1	16.0	24.0	Q2
MSP430F2618TPMR	LQFP	PM	64	1000	330.0	24.4	13.0	13.0	2.1	16.0	24.0	Q2
MSP430F2618TPNR	LQFP	PN	80	1000	330.0	24.4	15.0	15.0	2.1	20.0	24.0	Q2
MSP430F2618TZCAR	NFBGA	ZCA	113	2500	330.0	16.4	7.3	7.3	1.5	12.0	16.0	Q1
MSP430F2618TZQWR	BGA MICROSTAR JUNIOR	ZQW	113	2500	330.0	16.4	7.3	7.3	1.5	12.0	16.0	Q1
MSP430F2619TPMR	LQFP	PM	64	1000	330.0	24.4	13.0	13.0	2.1	16.0	24.0	Q2
MSP430F2619TPMR	LQFP	PM	64	1000	330.0	24.4	13.0	13.0	2.1	16.0	24.0	Q2
MSP430F2619TPNR	LQFP	PN	80	1000	330.0	24.4	15.0	15.0	2.1	20.0	24.0	Q2
MSP430F2619TZCAR	NFBGA	ZCA	113	2500	330.0	16.4	7.3	7.3	1.5	12.0	16.0	Q1
MSP430F2619TZQWR	BGA MICROSTAR JUNIOR	ZQW	113	2500	330.0	16.4	7.3	7.3	1.5	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS

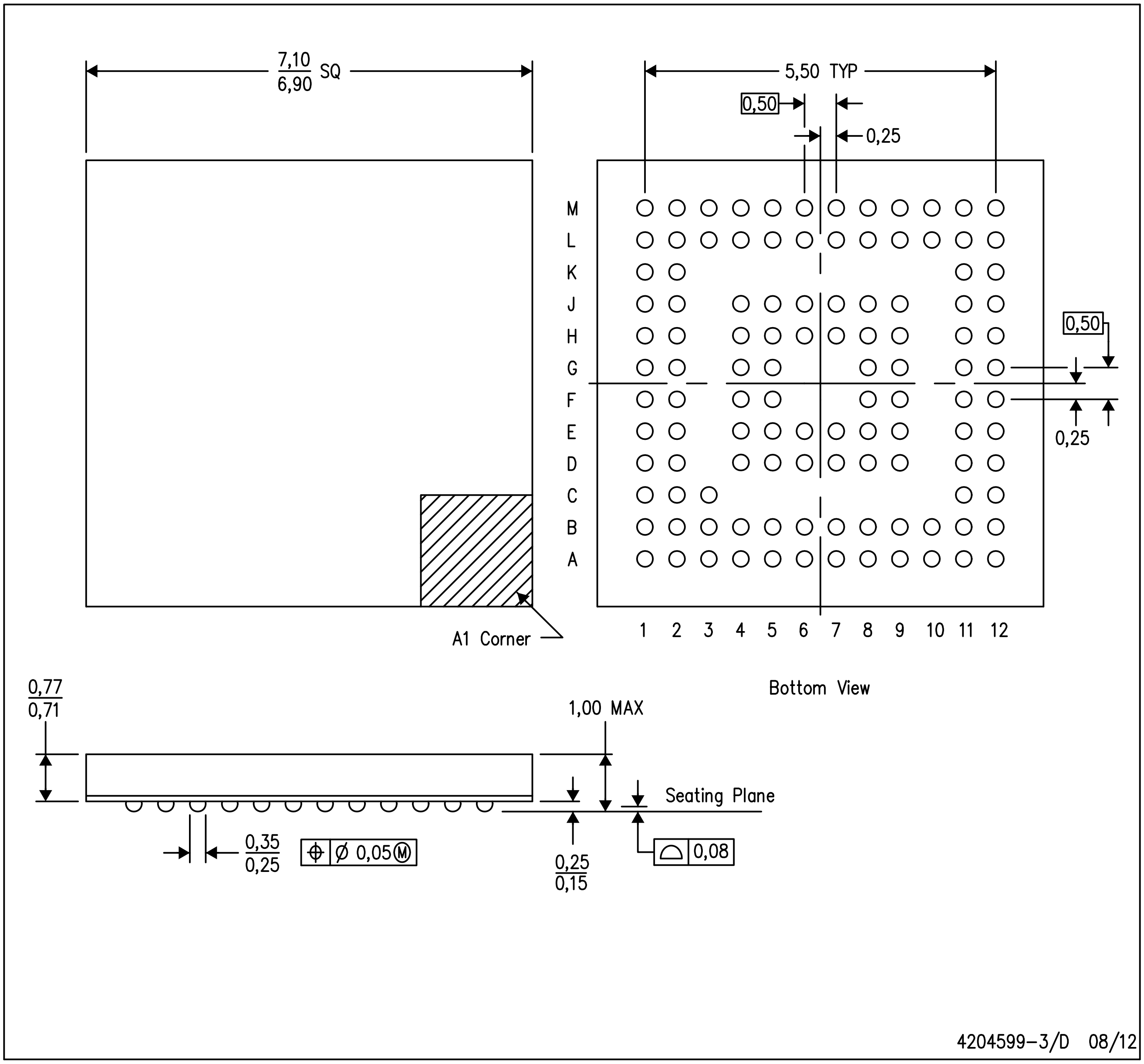


*All dimensions are nominal

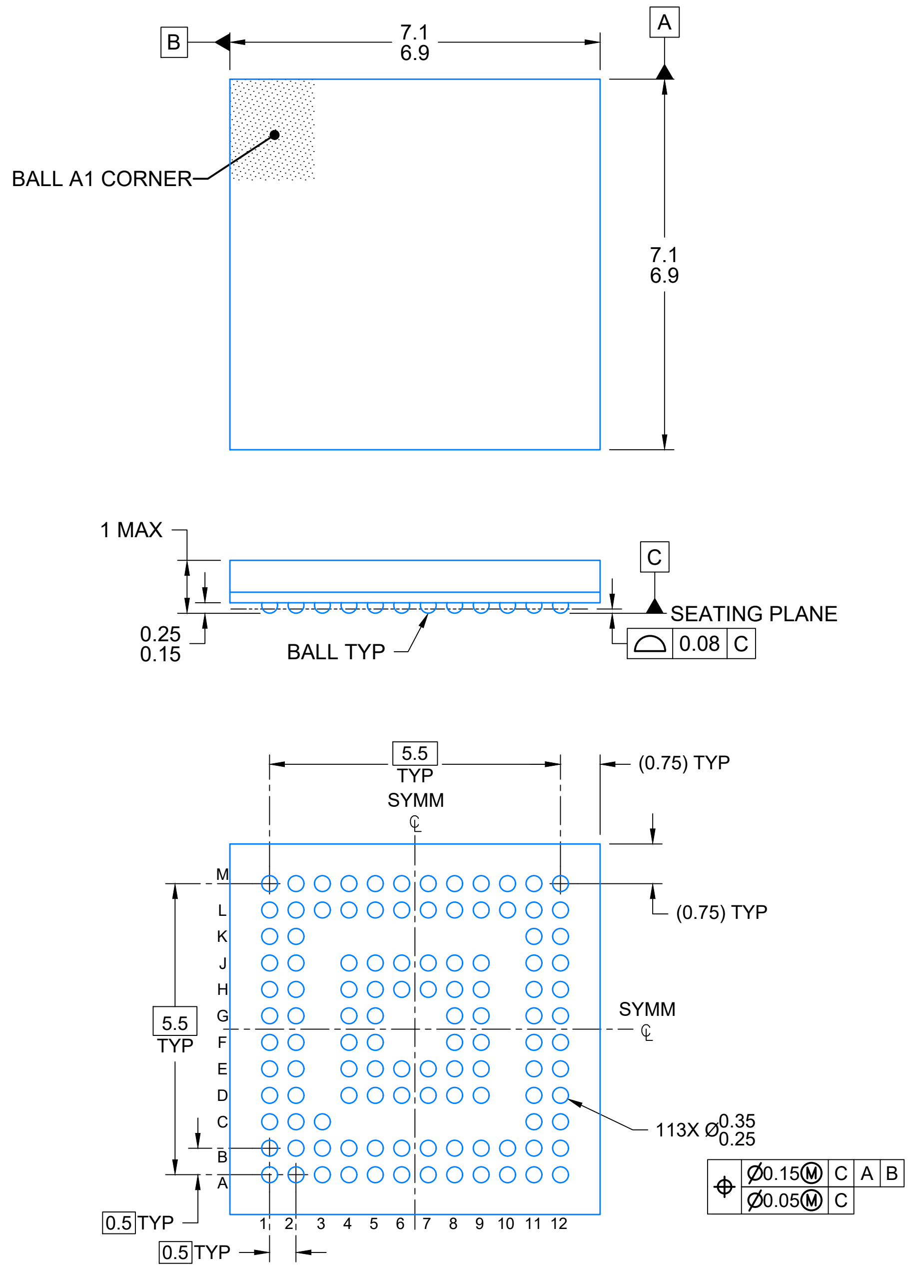
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
MSP430F2416TPMR	LQFP	PM	64	1000	350.0	350.0	43.0
MSP430F2416TPMR	LQFP	PM	64	1000	336.6	336.6	41.3
MSP430F2416TPNR	LQFP	PN	80	1000	350.0	350.0	43.0
MSP430F2416TZCAR	NFBGA	ZCA	113	2500	350.0	350.0	43.0
MSP430F2416TZQWR	BGA MICROSTAR JUNIOR	ZQW	113	2500	350.0	350.0	43.0
MSP430F2417TPMR	LQFP	PM	64	1000	350.0	350.0	43.0
MSP430F2417TPMR	LQFP	PM	64	1000	336.6	336.6	41.3
MSP430F2417TPNR	LQFP	PN	80	1000	350.0	350.0	43.0
MSP430F2417TZCAR	NFBGA	ZCA	113	2500	350.0	350.0	43.0
MSP430F2417TZQWR	BGA MICROSTAR JUNIOR	ZQW	113	2500	350.0	350.0	43.0
MSP430F2418TPMR	LQFP	PM	64	1000	336.6	336.6	41.3
MSP430F2418TPMR	LQFP	PM	64	1000	350.0	350.0	43.0
MSP430F2418TPNR	LQFP	PN	80	1000	350.0	350.0	43.0
MSP430F2418TZCAR	NFBGA	ZCA	113	2500	350.0	350.0	43.0
MSP430F2418TZQWR	BGA MICROSTAR JUNIOR	ZQW	113	2500	350.0	350.0	43.0
MSP430F2419TPMR	LQFP	PM	64	1000	350.0	350.0	43.0
MSP430F2419TPMR	LQFP	PM	64	1000	336.6	336.6	41.3
MSP430F2419TPNR	LQFP	PN	80	1000	350.0	350.0	43.0

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
MSP430F2419TZQWR	BGA MICROSTAR JUNIOR	ZQW	113	2500	350.0	350.0	43.0
MSP430F2616TPMR	LQFP	PM	64	1000	350.0	350.0	43.0
MSP430F2616TPMR	LQFP	PM	64	1000	336.6	336.6	41.3
MSP430F2616TPNR	LQFP	PN	80	1000	350.0	350.0	43.0
MSP430F2616TZCAR	NFBGA	ZCA	113	2500	350.0	350.0	43.0
MSP430F2616TZQWR	BGA MICROSTAR JUNIOR	ZQW	113	2500	350.0	350.0	43.0
MSP430F2617TPMR	LQFP	PM	64	1000	336.6	336.6	41.3
MSP430F2617TPMR	LQFP	PM	64	1000	350.0	350.0	43.0
MSP430F2617TPNR	LQFP	PN	80	1000	350.0	350.0	43.0
MSP430F2617TZCAR	NFBGA	ZCA	113	2500	350.0	350.0	43.0
MSP430F2617TZQWR	BGA MICROSTAR JUNIOR	ZQW	113	2500	350.0	350.0	43.0
MSP430F2618TPMR	LQFP	PM	64	1000	336.6	336.6	41.3
MSP430F2618TPMR	LQFP	PM	64	1000	350.0	350.0	43.0
MSP430F2618TPNR	LQFP	PN	80	1000	350.0	350.0	43.0
MSP430F2618TZCAR	NFBGA	ZCA	113	2500	350.0	350.0	43.0
MSP430F2618TZQWR	BGA MICROSTAR JUNIOR	ZQW	113	2500	350.0	350.0	43.0
MSP430F2619TPMR	LQFP	PM	64	1000	350.0	350.0	43.0
MSP430F2619TPMR	LQFP	PM	64	1000	336.6	336.6	41.3
MSP430F2619TPNR	LQFP	PN	80	1000	350.0	350.0	43.0
MSP430F2619TZCAR	NFBGA	ZCA	113	2500	350.0	350.0	43.0
MSP430F2619TZQWR	BGA MICROSTAR JUNIOR	ZQW	113	2500	350.0	350.0	43.0

ZQW (S–PBGA–N113) PLASTIC BALL GRID ARRAY



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MO–225
D. This is a Pb–free solder ball design.



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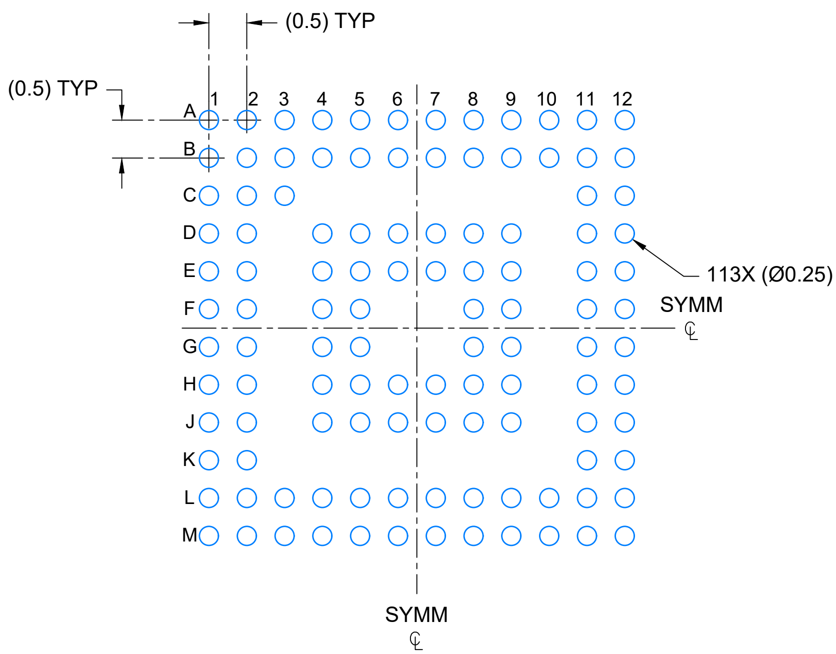
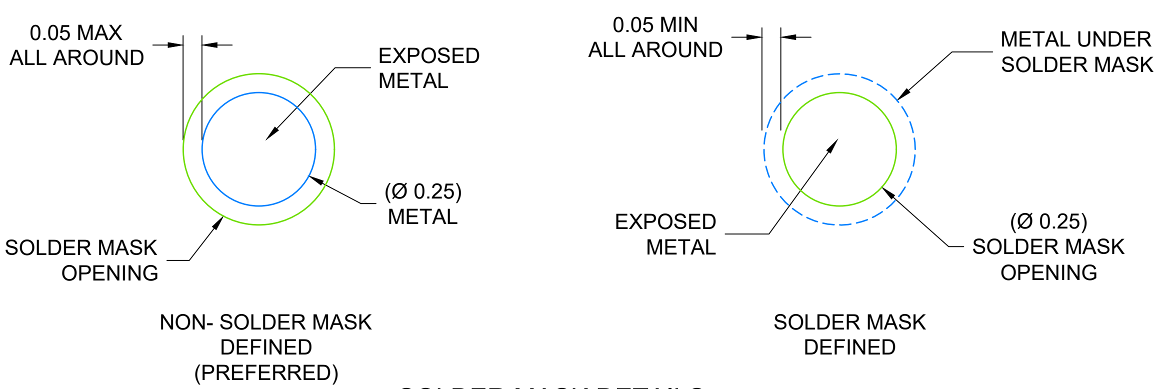
NOTES:

NanoFree is a trademark of Texas Instruments.

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
SCALE: 10X



SOLDER MASK DETAILS
NOT TO SCALE

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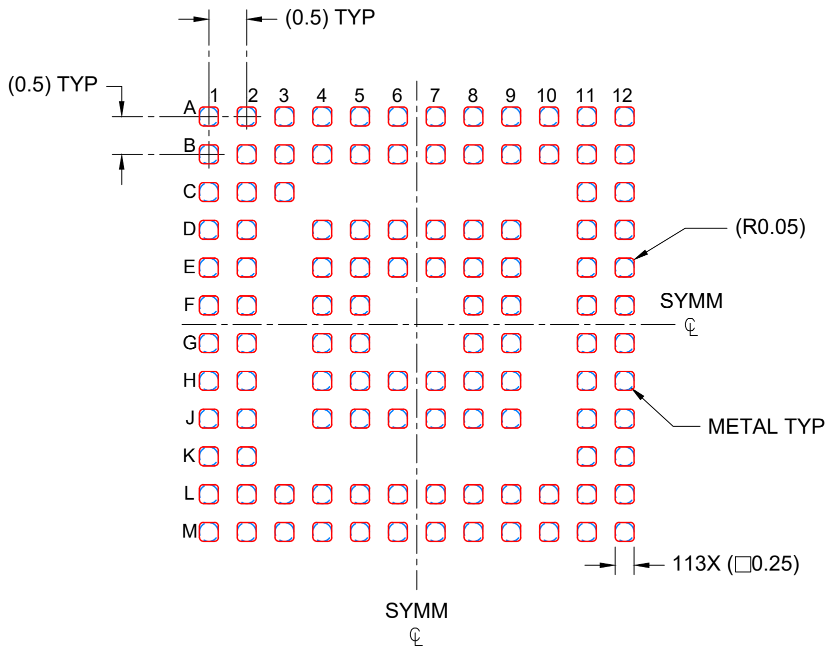
NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. Refer to Texas Instruments Literature number SNVA009 (www.ti.com/lit/snva009).



SOLDER PASTE EXAMPLE
BASED ON 0.100 mm THICK STENCIL
SCALE: 10X

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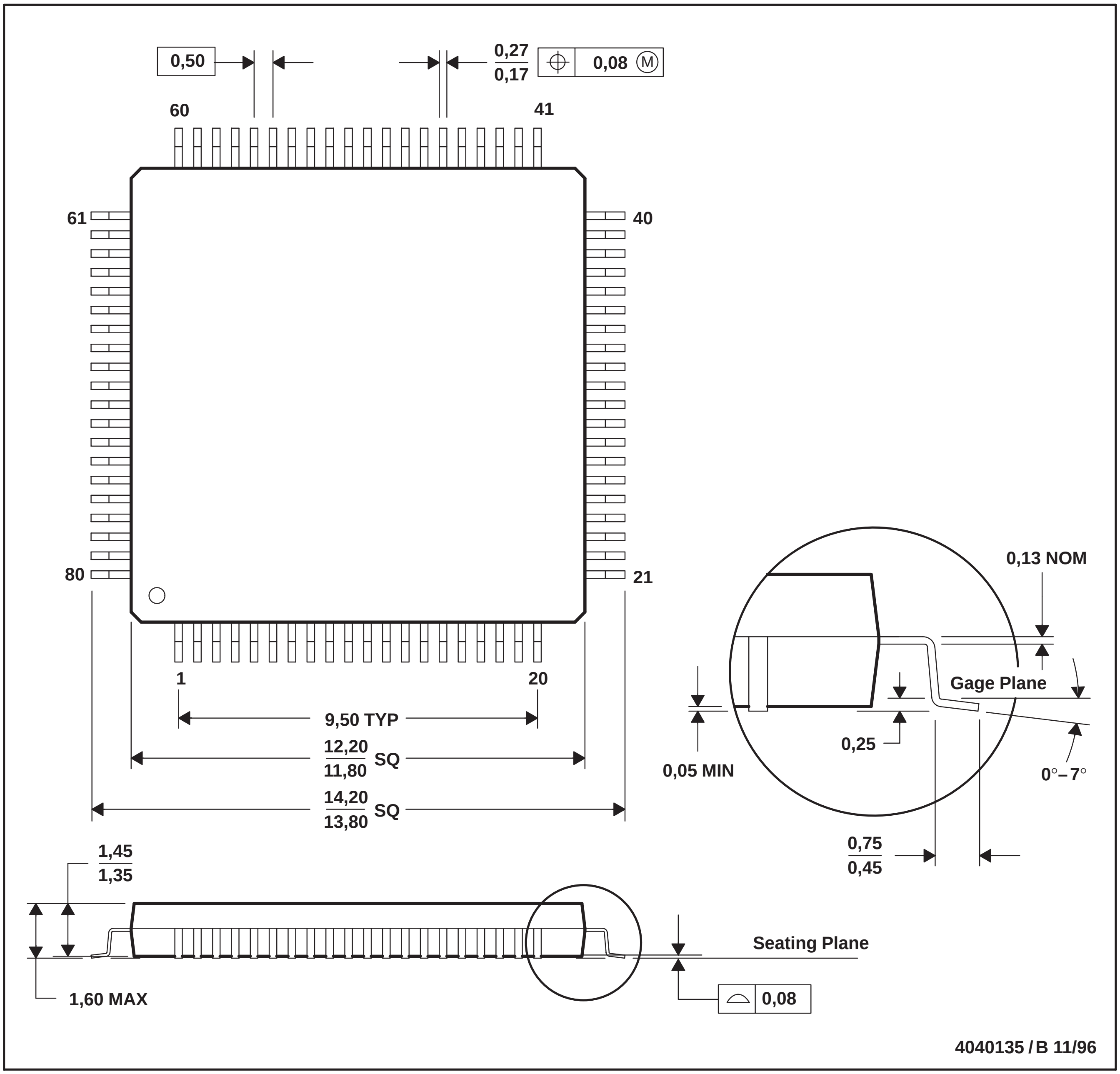
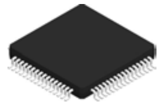
NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

PN (S-PQFP-G80) PLASTIC QUAD FLATPACK



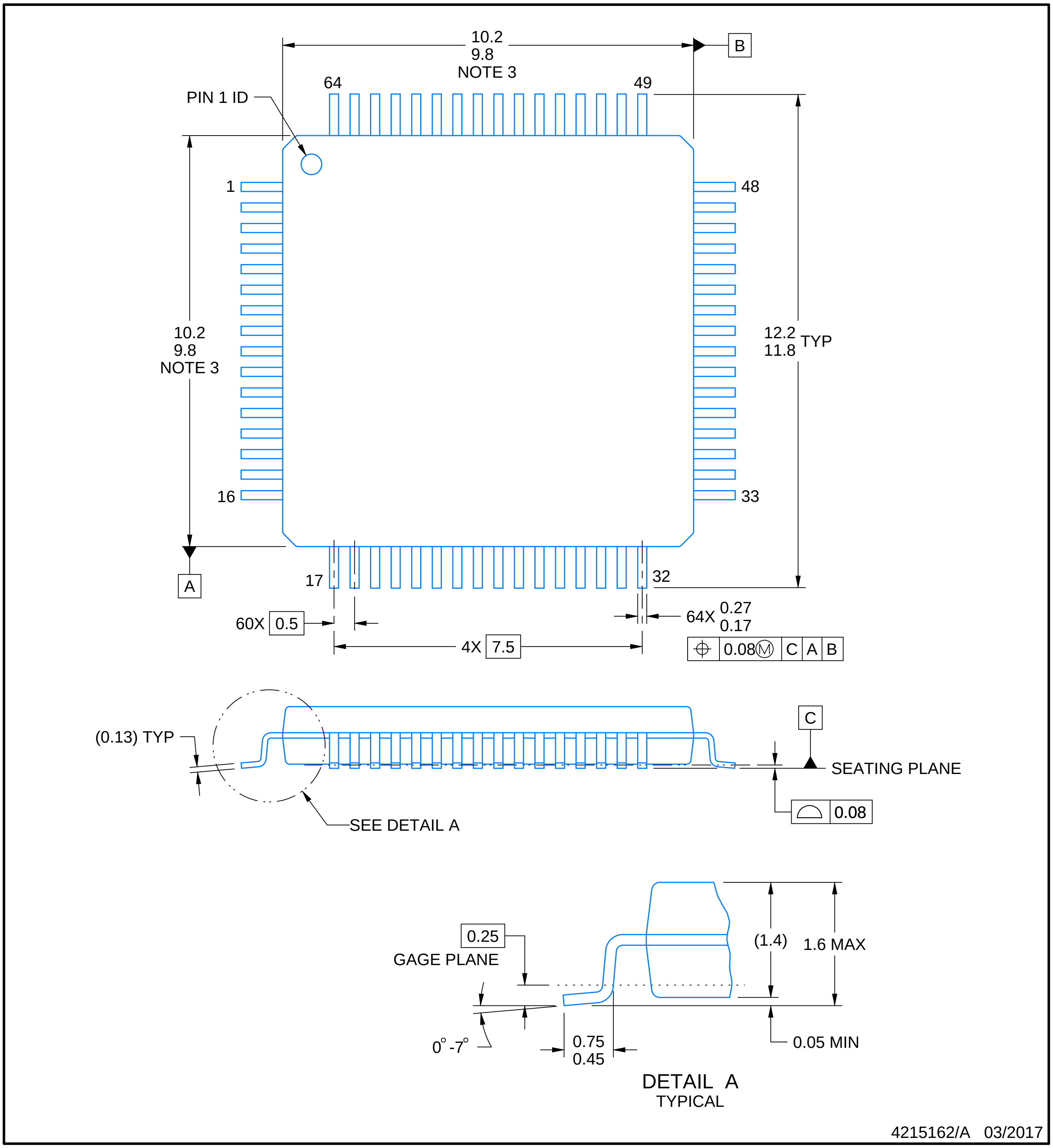
NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-026



PACKAGE OUTLINE

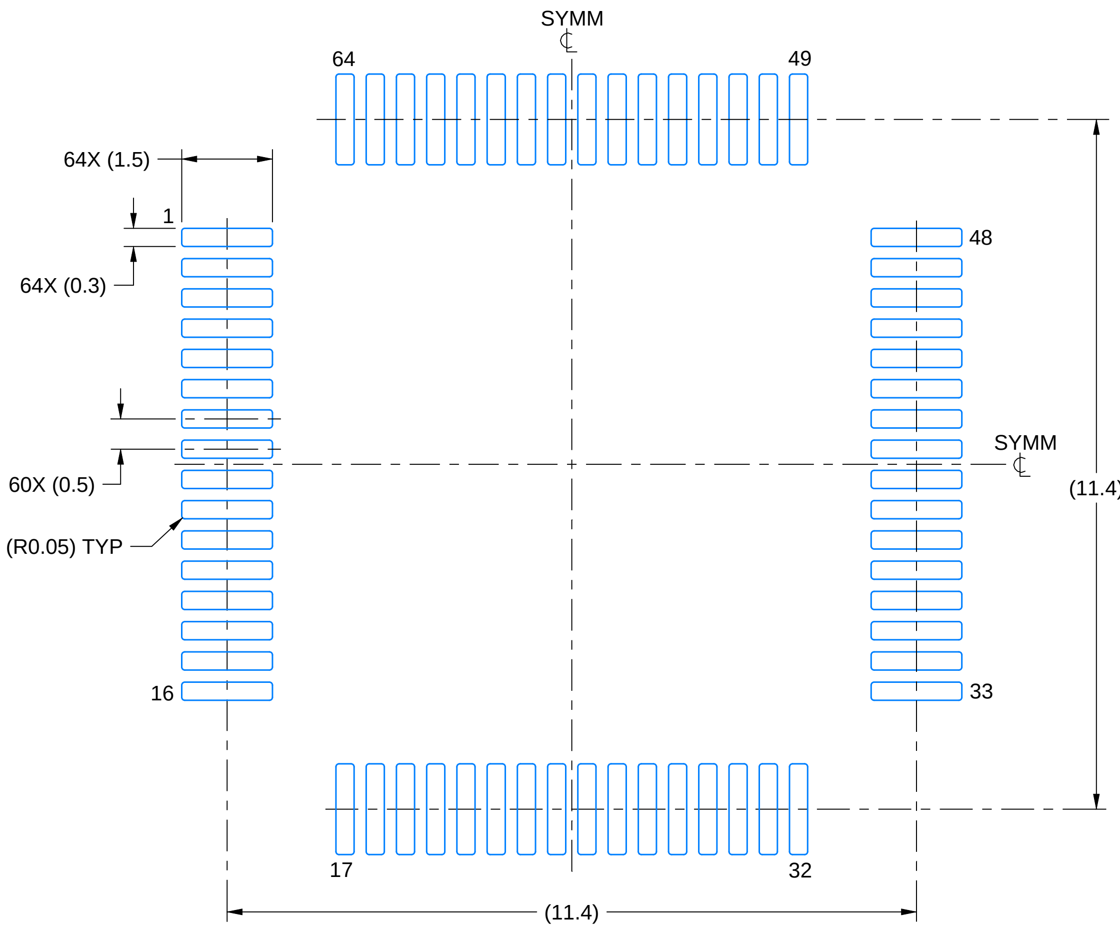
LQFP - 1.6 mm max height

PLASTIC QUAD FLATPACK

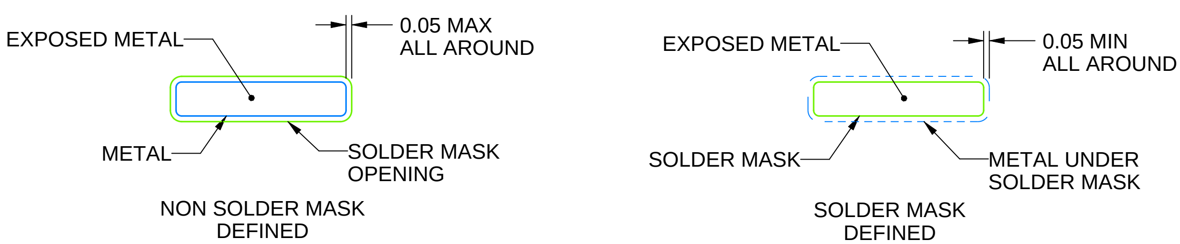


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MS-026.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X

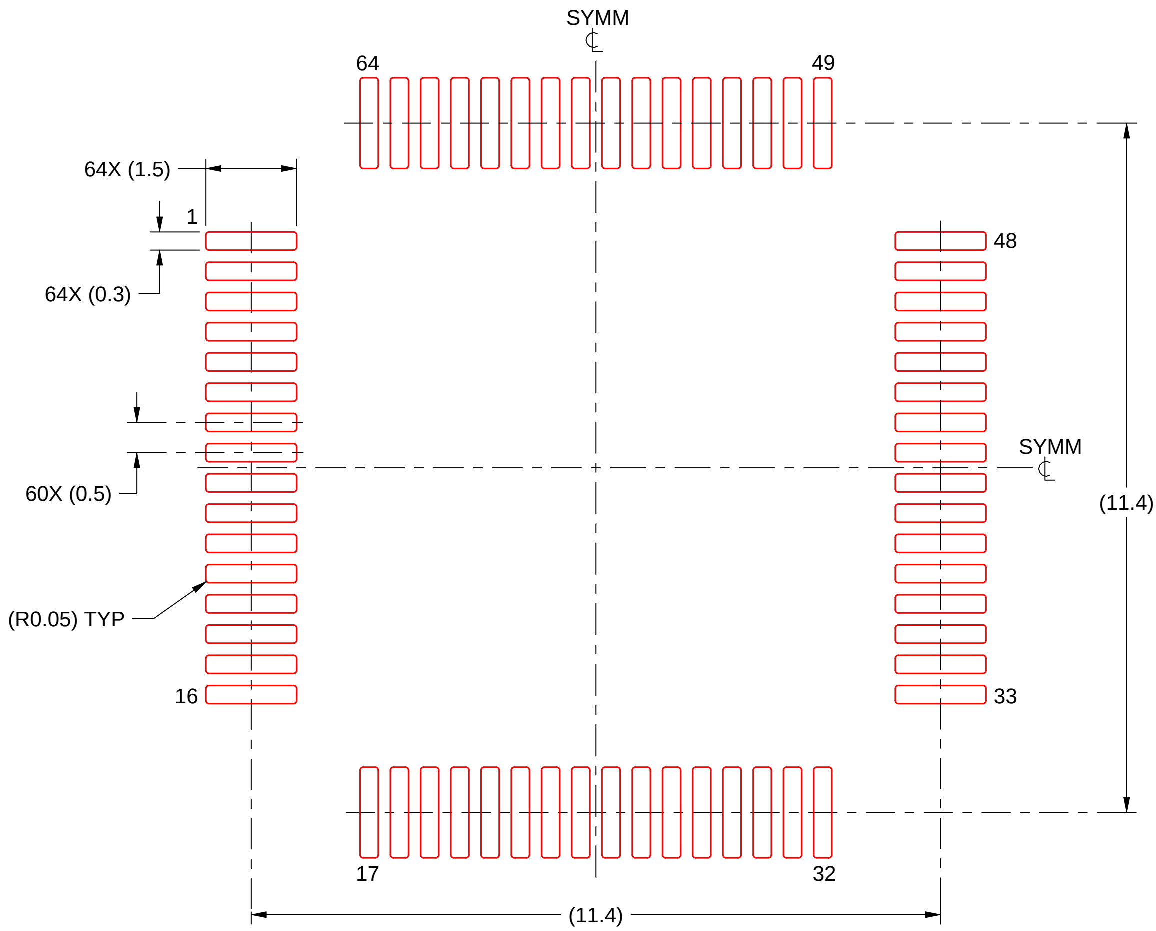


SOLDER MASK DETAILS

4215162/A 03/2017

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
7. For more information, see Texas Instruments literature number SLMA004 (www.ti.com/lit/slma004).



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4215162/A 03/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.