

RCL DISPLAY LTD.

DATA SHEET

LCD MODULE

MBC16263B SERIES

Product specification

Version : 0

05/Oct/2004

GENERAL SPECIFICATION

MODULE NO. :

MBC16263B SERIES

CUSTOMER P/N

VERSION NO.	CHANGE DESCRIPTION	DATE
0	ORIGINAL VERSION	2004/10/05

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DATE: 2004/10/05

CONTENTS


1. FUNCTIONS & FEATURES -----	2
2. MECHANICAL SPECIFICATIONS -----	2
3. BLOCK DIAGRAM -----	2
4. EXTERNAL DIMENSIONS-----	3
5. PIN ASSIGNMENT -----	3
6.1 PCB DRAWING AND DESCRIPTION -----	4
6.2 EXAMPLE APPLICATION -----	4
7. BACKLIGHT ELECTRICAL/OPTICAL SPECIFICATIONS-----	5
8. DISPLAY DATA RAM (DDRAM) -----	6
9. INSTRUCTION DESCRIPTION -----	6
10. INTERFACE WITH MPU IN BUS MODE -----	10
11. INITIALIZING BY INSTRUCTION -----	11
12. MAXIMUM ABSOLUTE POWER RATINGS-----	13
13. ELECTRICAL CHARACTERISTICS-----	13
14. CHARACTR GENERATOR ROM (S6A0070)-----	17
15. FRAME FREQUENCY -----	18
16. THE MODULE ACCEPT QUALITY LEVEL (AQL)-----	19
17. RELIABILITY TEST-----	19
18. LCD MODULES HANDLING PRECAUTIONS -----	20
19. OTHERS -----	20

1. FUNCTIONS & FEATURES


- MBC16263B Series LCD type :

MODULE	LCD MODEL	LCD TYPE
MBC16263B00	DC16220E09	STN Blue Transmissive Negative Mode

- Viewing Direction : 6 O'clock (**Remark:** The LCD wiring is symmetrical and thus LCD can be used as 12 O'clock and 6 O'clock with physical change of direction of the LCD. The LCD is placed as following)



Viewing Direction: 12 O'clock

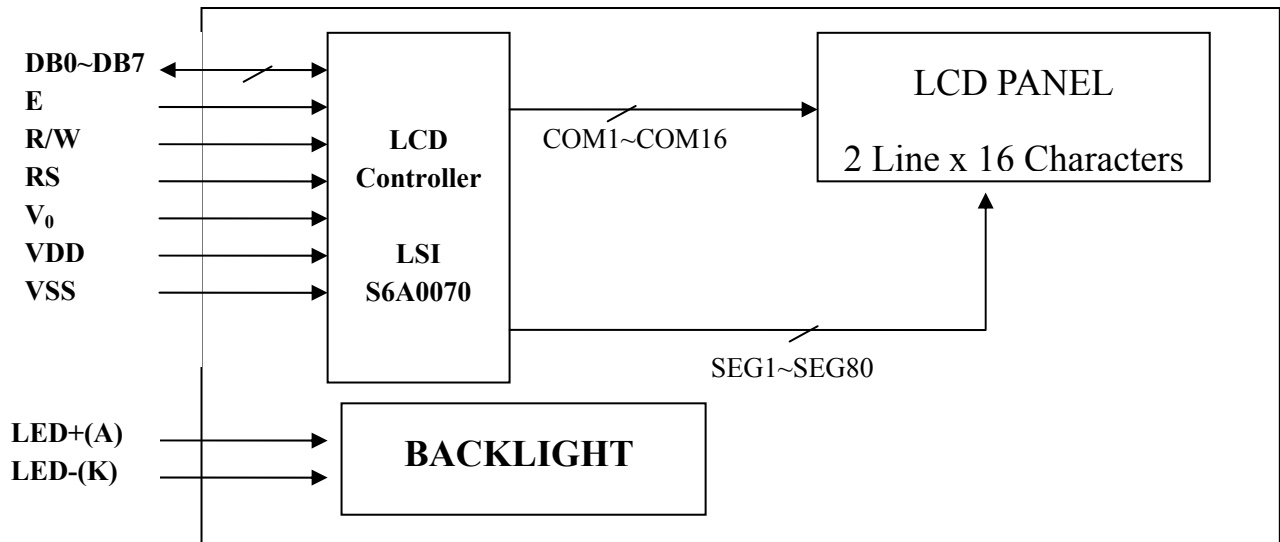


Viewing Direction: 6 O'clock
- Driving Scheme : 1/16 Duty Cycle, 1/5 Bias
- Power Supply Voltage : 2.7 to 5.5V (typical 5.0V)
- Backlight Color : White
- V_{LCD} Adjustable For Best Contrast : 4.5V
- Display contents : 16 x 2 Characters (5 x 8 dots, Format : 192 Kinds)
- Internal Memory : CGROM (8,320 bits)
: CGRAM (64 x 8 bits)
: DDRAM (80 x 8 bits for 80 Digits)
- Easy Interface with a 4-bit or 8-bit MPU

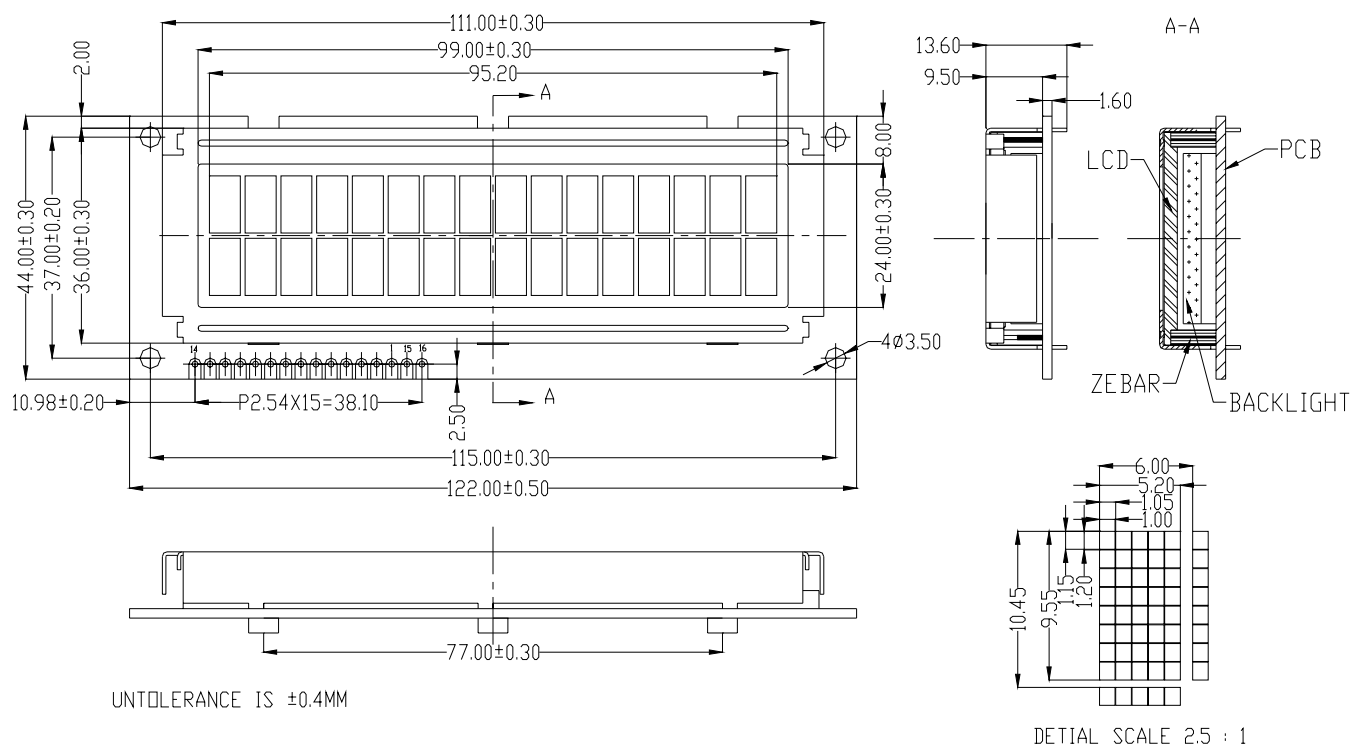
2. MECHANICAL SPECIFICATIONS

- Character Pitch : 6.00 (W) x 10.45 (H) mm
- Character Size : 5.20 (W) x 9.55 (H) mm
- Character Font : 5 x 8 dots
- Dot Size : 1.00 (W) x 1.15 (H) mm
- Dot Pitch : 1.05 (W) x 1.20 (H) mm

3. BLOCK DIAGRAM



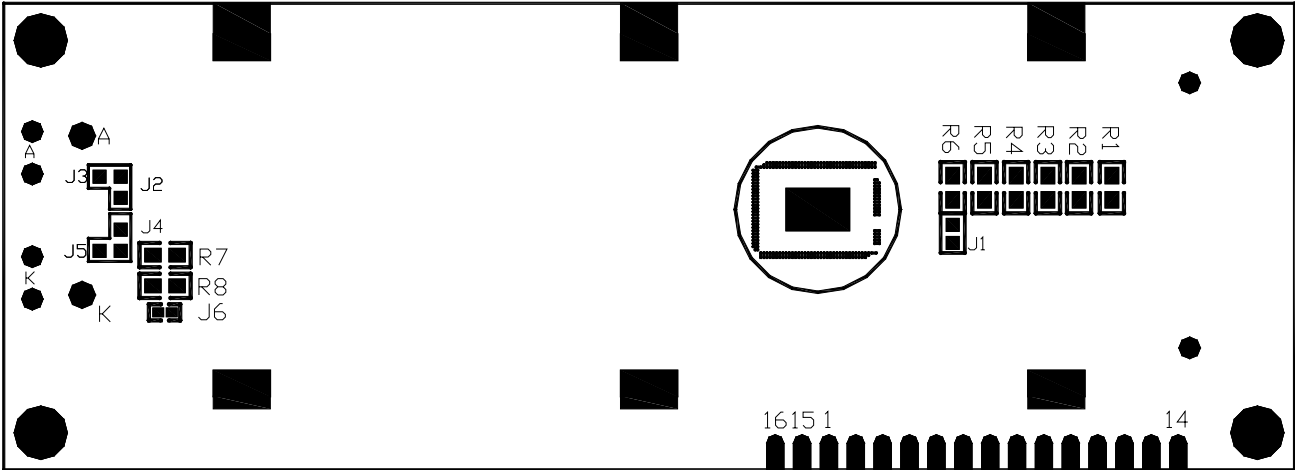
4. EXTERNAL DIMENSIONS



5. PIN ASSIGNMENT

Pin No.	Symbol	Function
1	VSS	Ground terminal of module.
2	VDD	Supply terminal of module 5.0V
3	V0	Power Supply for liquid crystal drive.
4	RS	Register select RS = 0...Instruction register RS = 1...Data register
5	R/W	Read /Write R/W = 1...Read R/W = 0...Write
6	E	Enable
7	DB0	Bi-directional data bus, data transfer is performed once, thru DB0 to DB7, in the case of interface data. Length is 8-bits; and twice, thru DB4 to DB7 in the case of interface data length is 4-bits. Upper four bits first then lower four bits.
8	DB1	
9	DB2	
10	DB3	
11	DB4	
12	DB5	
13	DB6	
14	DB7	
15	LED - (K)	Please also refer to 6.1 PCB drawing and description.
16	LED + (A)	

6. 1PCB DRAWING AND DESCRIPTION



DESCRIPTION:

6-1-1.The polarity of the pin 15 and the pin 16:

symbol	state	symbol	J3,J5	J2, J4	LED Polarity	
					15 Pin	16 Pin
J2,J4	Each solder-bridge		Each open	Each closed	Anode	Cathode
J3,J5	Each solder-bridge		Each closed	Each open	Cathode	Anode

Note: In application module, J3=J5=closed, J2=J4=open

6-1-2. The metal-bezel is set on ground when the J1 is closed

Note: In application module, J1=closed.

6-1-3.The LED resistor should can be bridged when the J6 is closed

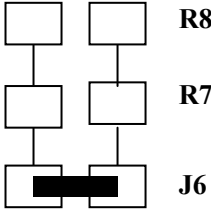
Note: In application module, J6=open

6-1-4.The R7 and the R8 are the LED resistor.

Note: In application module, R7=R8=33 Ω

6.2 Example application

6-2-1. The LED resistor should be bridged as following.



6-2-2. The 15 pin is the anode and the 16 pin is the cathode as following.



6-2-3. The 15 pin is the cathode and the 16 pin is the anode as following.



6-2-4. The metal-bezel is on ground as following.



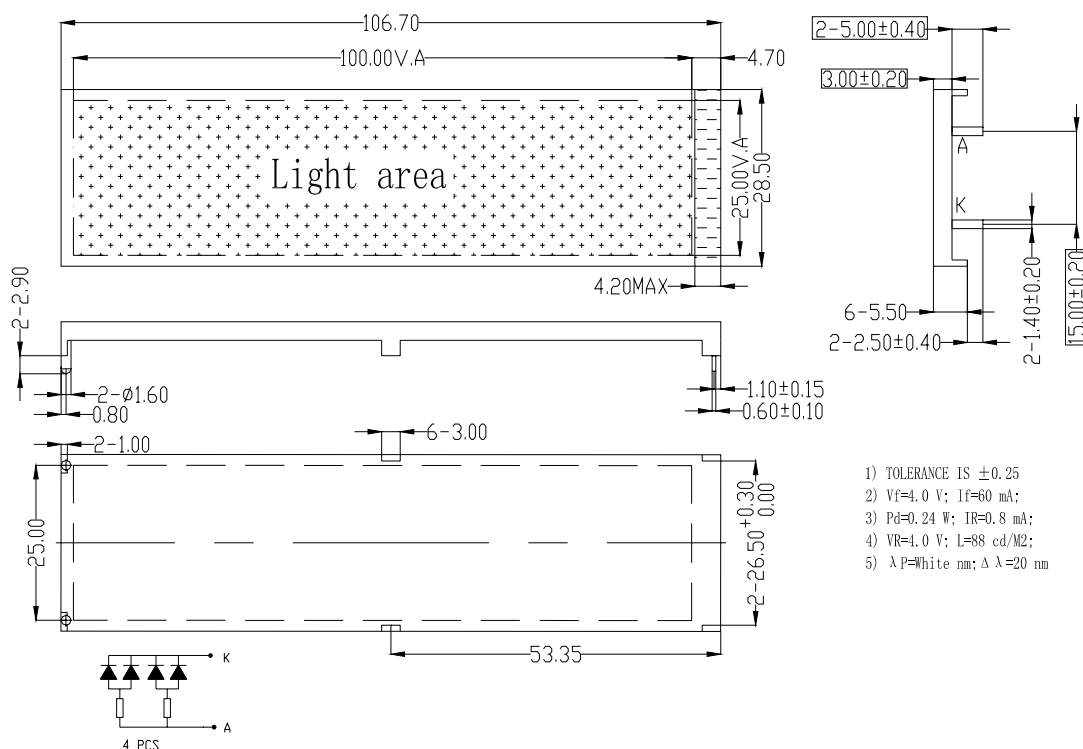
7. BACKLIGHT & SWITCH (Ta=-20~+70℃)

7-1 For MBC16263B00

Item	Symbol	Min	Typ	Max	Unit	Conditions
Forward Voltage	Vf		4.0	4.2	V	
Forward Current	If		60	80	mA	Vf=4.0V
Power Dissipation	Pd		0.24		W	Vf=4.0V
Reverse Voltage	VR		4		V	
Reverse Current	IR		0.8		mA	
Luminous Intensity	IV	65	88		Cd/m ²	Vf=4.0V
Luminous Uniformity		70			%	
Emission Wavelength	λ p		white		nm	If=20mA Ta=25℃ Each chip
Chromaticity Coordinate		X=0.270 Y=0.275		X=0.315 Y=0.32		If=70mA
Spectral Range	△ λ		20		nm	℃

	Symbol	Ratings
Operating Temperature	Topr	-20℃ to +70℃
	Tstg	-30℃ to +80℃

7-2. Backlight Package Dimensions & Circuit Diagram.



8. DISPLAY DATA RAM (DDRAM)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	
FIRST LINE	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	← Display position ← DDRAM Address
SECOND LINE	40	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E	4F	

9. INSTRUCTION DESCRIPTION

Outline

To overcome the speed difference between the internal clock of S6A0070 and the MPU clock, S6A0070 performs internal operations by storing control information to IR or DR. The internal operation is determined according to the signal from MPU, composed of read/write and data bus (refer to table 5.)

Instruction can be divided largely into four kinds:

- (1) S6A0070 function set instructions (set display methods, set data length, etc.)
- (2) Address set instructions to internal RAM.
- (3) Data transfer instructions with internal RAM.
- (4) Others.

The address of the internal RAM is automatically increased or decreased by 1.

*NOTE: During internal operation, busy flag (DB7) is read"1". Busy flag check must be preceded by the next instruction.

When you make an MPU program with checking the busy flag (DB7), it must be necessary 1/2 fosc for executing the next instruction by falling E signal after the busy flag (DB7) goes to "0".

Contents

1) Clear display

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	0	0	1

Clear all the display data by writing "20H"(space code) to all DDRAM address, and set the DDRAM addresses to "00H" in the AC (address counter). Return cursor to original status, namely, bring the cursor to the left edge on first line of the display. Make entry mode increment (I/D="1").

2) Return home

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	0	1	x

Return home is the cursor return home instruction.

Set DDRAM address to "00H" in the address counter. Return cursor to its original site and return display to its original status, if shifted. Contents of DDRAM does not change.

3) Entry mode set

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	1	I/D	SH

Set the moving direction of cursor and display.

I/D: increment/decrement of DDRAM address is increased by 1.

When I/D="1", cursor/blink moves to right and DDRAM address is increased by 1.

When I/D="0", cursor/blink moves to left and DDRAM address is increased by 1.

CGRAM operates the same as DDRAM, when reading from or writing to CGRAM.

SH: shift of entire display

When DDRAM is in read (CGRAM read/write) operation or SH="0", shift of entire display is not performed.

If SH="1" and in DDRAM write operation, shift of entire display is performed according to I/D value (I/D="1": shift left, I/D="0": shift right).

4) Display ON/OFF control

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	1	D	C	B

Control display/cursor/blink ON/OFF 1-bit register.

D: Display ON/OFF control bit

When D="1", entire display is turned on.

When D="0", display is turned off, but display data remains in DDRAM.

C: cursor or ON/OFF control bit

When C="1", cursor is turned on.

When C="0", cursor disappears in current display, but I/D register retains its data.

B: cursor blink ON/OFF control bit

When B="1", cursor blink is on, which performs alternately between all the "1" data and display characters at the cursor position.

When B="0", blink is off

5) Cursor or display shift

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	1	S/C	R/L	X	X

Without writing or reading the display data, shift right/left cursor position or display.

This instruction is used to correct or search display data. (refer to table 40)

During 2-line mode display, cursor moves to the 2nd line after the 40th digit of the 1st line.

Note that display shift is performed simultaneously in all the lines.

When displayed data is shifted repeatedly, each line shifts individually.

When display shift is performed, the contents of the address counter are not changed.

Table 4. shift patterns according to S/C and R/L bits

S/C	R/L	operation
0	0	Shift cursor to the left, AC is decreased by 1
0	1	Shift cursor to the right, AC is decreased by 1
1	0	Shift all the display to the left, cursor moves according to the display
1	1	Shift all the display to the right, cursor moves according to the display

6) Function set

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	DL	N	F	X	X

DL: Interface data length control bit

When DL="1", it means 8-bit bus mode with MPU.

When DL="0", it means 4-bit bus mode with MPU. So to speak, DL is a signal to select 8-bit or 4-bit bus mode.

When 4-bit bus mode, it needs to transfer 4-bit data in two parts.

N: display line number control bit

When N="0", it means 1-line display mode.

When N="1", it means 2-line display mode.

F: display font type control bit

When F="0", 5 x 7 dots format display mode.

When F="1", 5 x 10 dots format display mode.

7) Set CGRAM address

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	1	AC5	AC4	AC3	AC2	AC1	AC0

Set CGRAM address to AC.

This instruction makes CGRAM data available from MPU.

8) Set DDRAM address

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	AC6	AC5	AC4	AC3	AC2	AC1	AC0

Set DDRAM address to AC

This instruction makes DDRAM data available from MPU.

When in 1-line display mode (N=0), DDRAM address is from "00H" to "4FH".

In 2-line display mode (N=1), DDRAM address in the 1st line is from "00H" to "27H", and DDRAM address in the 2nd line is from "40H" to "67H".

9) Read busy flab & address

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	BF	AC6	AC5	AC4	AC3	AC2	AC1	AC0

This instruction shows whether S6A0070 is in internal operation or not. If the resultant BF is "1", it means the internal operation is in progress and you have to wait until BF is low. Then the next instruction can be performed. In this instruction you can also read the value of the address counter.

10) Write data to RAM

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	0	D7	D6	D5	D4	D3	D2	D1	D0

Write binary 8-bit data to DDRAM / CGRAM

The selection of RAM from DDRAM, and CGRAM, is set by the previous address set instruction: DDRAM address set, and CGRAM address set. RAM set instruction can also determine the AC direction to RAM.

After write operation, the address is automatically increased/decreased by 1, according to the entry mode.

11) Read data to RAM

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	1	D7	D6	D5	D4	D3	D2	D1	D0

Read binary 8-bit data from DDRAM/CGRAM.

The selection of RAM is set by the previous address set instruction. If the address set instruction of RAM is not performed before this instruction, the data that is read first is invalid, because the direction of AC is not determined. If you read RAM data several times without RAM address set instruction before read operation, you can get correct RAM data. In the case of DDRAM read operation, cursor shift instruction plays the same role as DDRAM address set instruction; it also transfers RAM data to the output data register.

After read operation the address counter is automatically increased/decreased by 1 according to the entry mode. After CGRAM read operation, display shift may not be executed correctly.

In the case of RAM write operation, after this AC is increased/decreased by 1 like read operation. At his time, AC indicates the next address position, but your can read only the previous data by the read instruction.

Table 5.instruction table

Instruction	Instruction Code										Description	Execution time (fosc=270kHz)
	R S	R/ W	DB 7	DB 6	DB 5	DB 4	DB 3	DB 2	DB 1	DB 0		
Clear Display	0	0	0	0	0	0	0	0	0	1	Write "20H" to DDRAM and set DDRAM address to "00H" from AC.	1.53 ms
Return Home	0	0	0	0	0	0	0	0	1	x	Set DDRAM address to "00H" from AC and return cursor to its original position if shifted.	1.53ms
Entry Mode set	0	0	0	0	0	0	0	1	I/D	SH	Assign cursor moving direction and enable the shift of entire display.	39us
Display ON/OFF Control	0	0	0	0	0	0	1	D	C	B	Set display (D), cursor(C), and blinking of cursor (B) on/off control bit.	39us
Cursor or Display shift	0	0	0	0	0	1	S/C	R/L	X	X	Set cursor moving and display shift control bit, and the direction without changing of DDRAM data.	39us
Function set	0	0	0	0	1	DL	N	F	X	X	Set interface data length (DL:4-bit/8-bit), numbers of display line (N:1-line/2-line, display font type (F:0...))	39us
Set CGRAM address	0	0	0	1	AC 5	AC 4	AC 3	AC 2	AC 1	AC 0	Set CGRAM address in address counter.	39us
Set CGRAM address	0	0	1	AC 6	AC 5	AC 4	AC 3	AC 2	AC 1	AC 0	Set DDRAM address in address counter.	39us
Read busy flag and address	0	1	BF	AC 6	AC 5	AC 4	AC 3	AC 2	AC 1	AC 0	Whether during internal operation or not can be known by reading BF. The contents of address counter can also be read.	0us
Write data to RAM	1	0	D7	D6	D5	D4	D3	D2	D1	D0	Write data into internal RAM (DDRAM/CGRAM).	43us
Read data to RAM	1	1	D7	D6	D5	D4	D3	D2	D1	D0	Read data into internal RAM (DDRAM/CGRAM).	43us

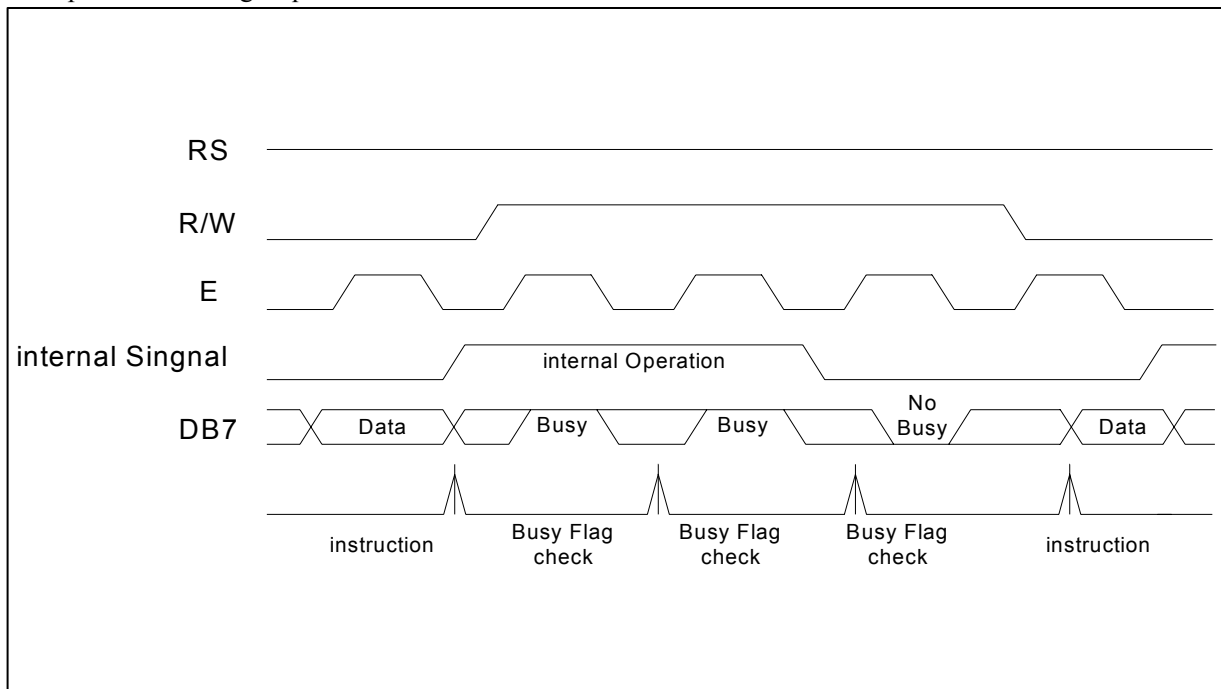
NOTE: when you make an MPU program with checking the busy flag (DB7), it must be necessary 1/2 Fosc for executing the next instruction by falling E signal after the busy flag (DB7) goes to "0".

10. INTERFACE WITH MPU IN BUS MODE

1) Interface with 8-bit MPU

When interfacing data length are 8-bit, transfer is performed all at once through 8-ports, from DB0 to DB7.

An example of the timing sequence is shown below.



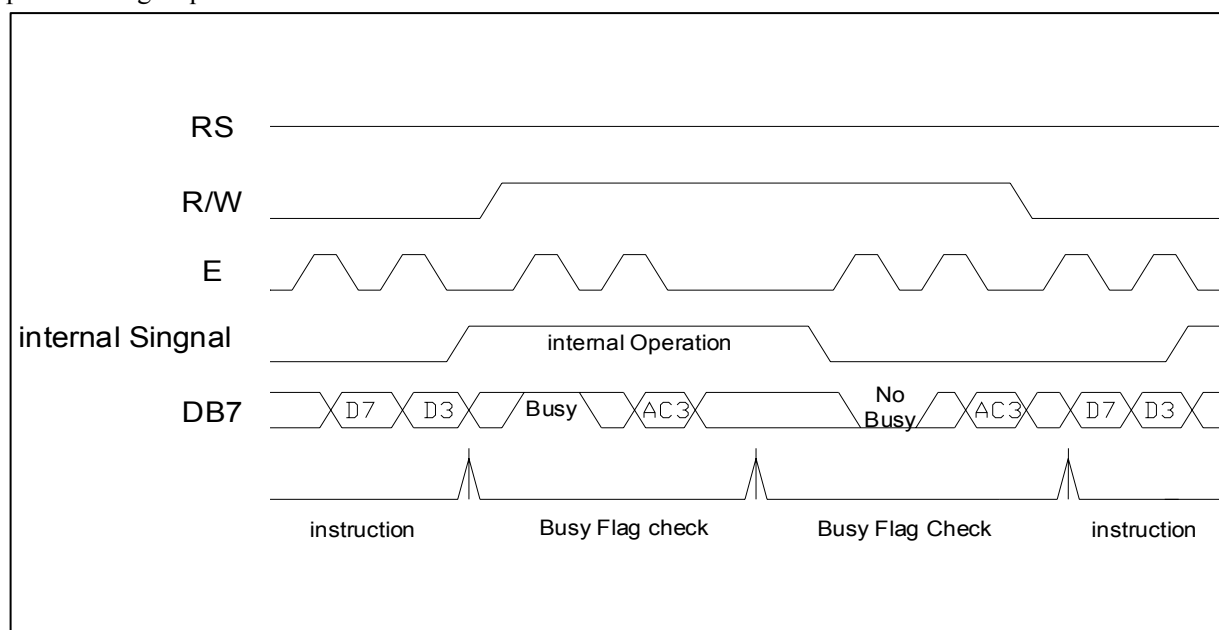
Example of 8-bit bus mode timing diagram

2) Interface with 4-bit MPU

When interfacing data length are 4-bit, only 4 ports, from DB4 to DB7, are used as data bus.

At first, higher 4-bit (in case of 8-bit bus mode, the contents of DB4 to DB7) are transferred, and then the lower 4-bit (in case of 8-bit bus mode, the contents of DB0 to DB3) are transferred. So transfer is performed in two parts. Busy flag outputs "1" after the second transfer are ended.

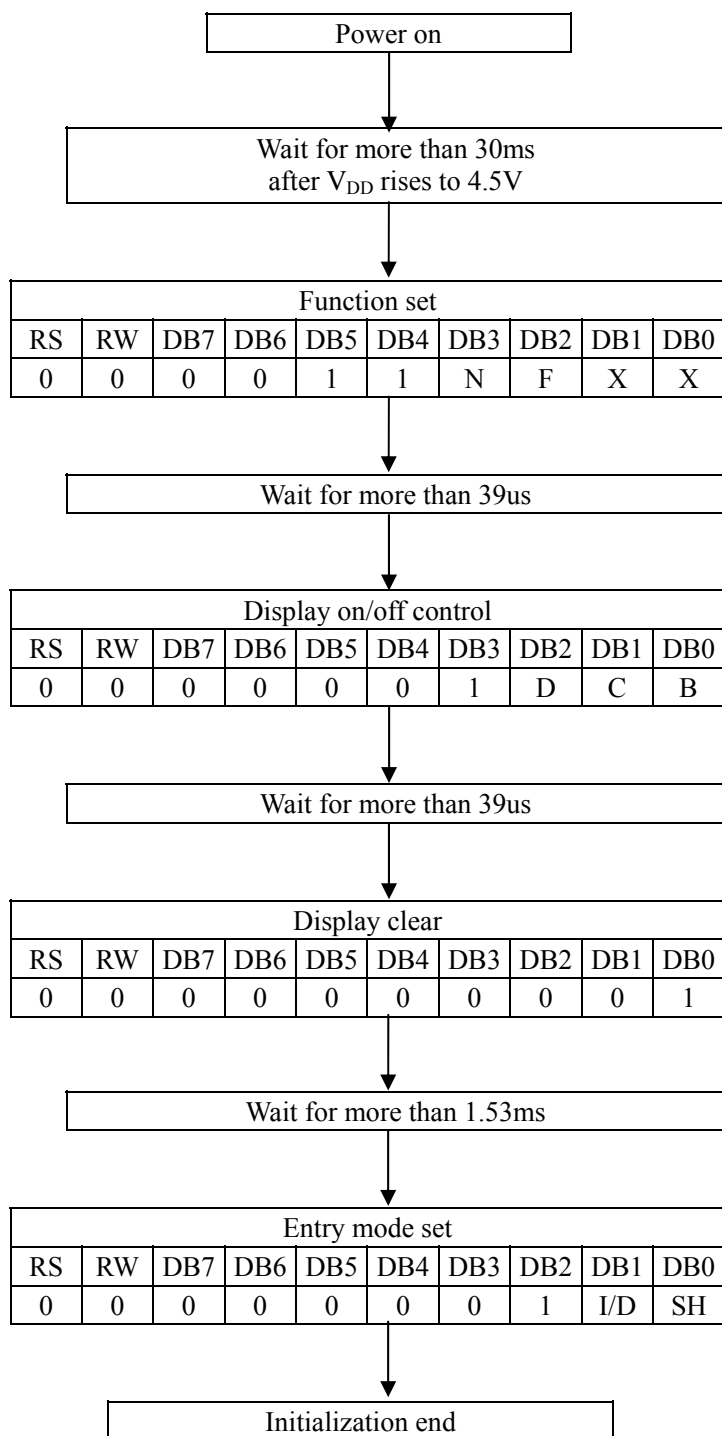
Example of timing sequence is shown below.



Example of 4-bit bus mode timing diagram

11. INITIALIZING BY INSTRUCTION

11-1. 8-bit interface mode



Condition : fosc=270khz

N	0	1-line mode
	1	2-line mode

F	0	5 x 7 dots
	1	5 x 10 dots

D	0	display off
	1	display on

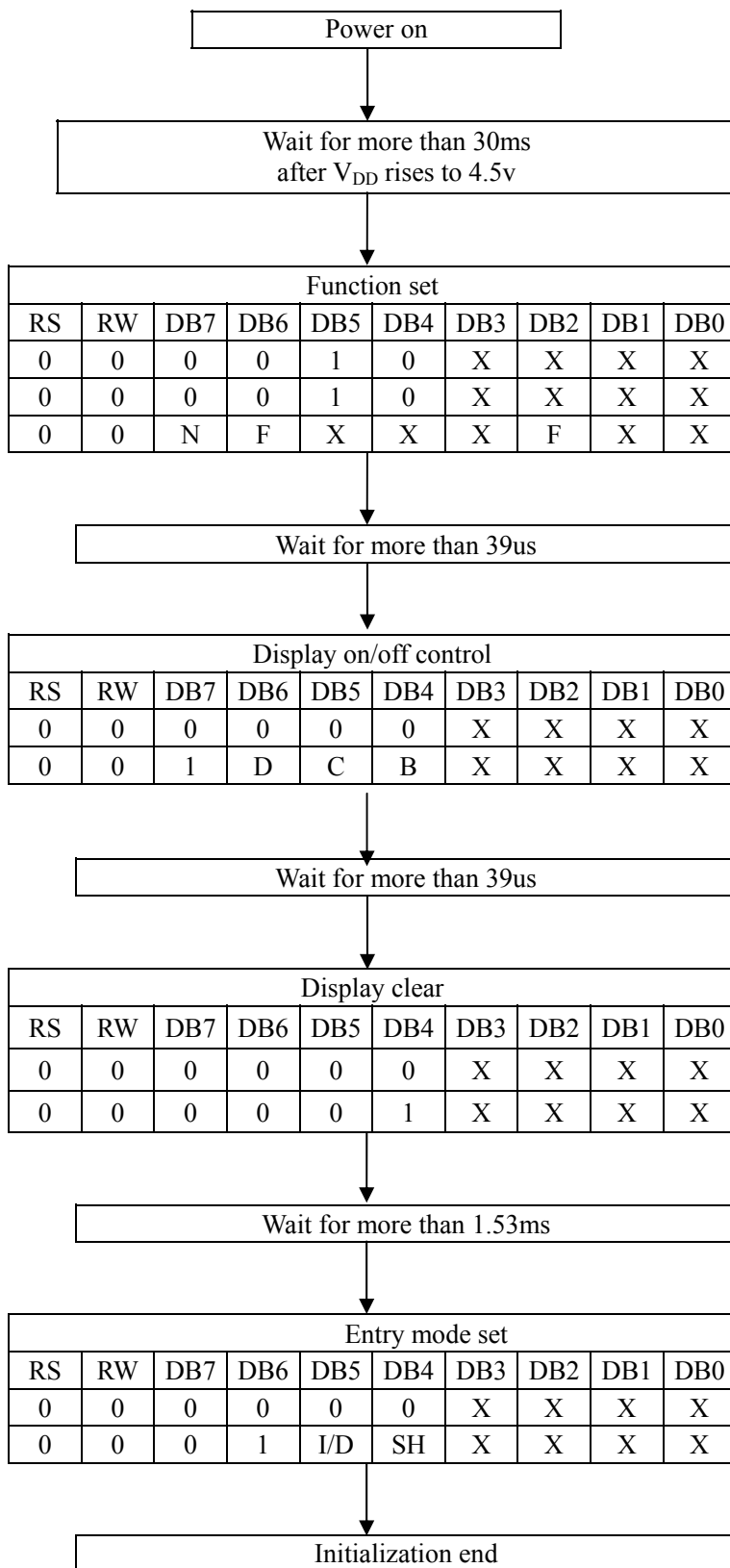
C	0	cursor off
	1	cursor on

B	0	blink off
	1	blink on

I/D	0	decrement mode
	1	increment mode

SH	0	entire shift off
	1	entire shift on

11-2. 4-bit interface mode



Condition : fosc=270khz

N	0	1-line mode
	1	2-line mode
F	0	5 x 7 dots
	1	5 x 10 dots

D	0	display off
	1	Display on
C	0	cursor off
	1	cursor on
B	0	blink off
	1	blink on

I/D	0	decrement mode
	1	increment mode
SH	0	entire shift off
	1	entire shift on

12. MAXIMUM ABSOLUTE POWER RATINGS(Ta=25°C)

Item	Symbol	Standard value	Unit
Power supply voltage(1)	V _{DD}	-0.3~+7.0	V
Power supply voltage(2)	V _{LCD}	V _{DD} -15.0~V _{DD} +0.3	V
Input voltage	V _{IN}	-0.3~V _{DD} +0.3	V
Operating temperature	Topr	-20~+70	°C
Storage temperature	Tstg	-30~+80	°C

13. ELECTRICAL CHARACTERISTICS
13-1 DC Characteristics(VDD=4.5V~5.5V,Ta=-20~+70°C)

Item	Symbol	Standard Value			Test Condition	Unit
		MIN	TYP	MAX		
Operating Voltage	V _{DD}	4.5	---	5.5	-----	V
Supply Current	I _{DD1}	----	0.7	1.0	Ceramic oscillation fosc=250kHz	mA
	I _{DD2}	----	0.4	0.6	Resistor oscillation external clock operation fosc=270kHz	
Input Voltage(1) (except OSC1)	V _{IL1}	-0.3	--	0.6	-----	V
	V _{IH1}	2.2	--	V _{DD}	-----	
Input Voltage(2) (OSC1)	V _{IL2}	-0.2	--	1.0	-----	V
	V _{IH2}	V _{DD} -1.0	--	V _{DD}	-----	
Output Voltage (1) (DB0 to DB7)	V _{OL1}	---	----	0.4	I _{OL} =1.2uA	V
	V _{OH1}	2.4	---	----	I _{OH} =-0.205mA	
Output Voltage (2) (except DB0 to DB7)	V _{OL2}	-----	---	0.1V _{DD}	I _{OL} =40uA	V
	V _{OH2}	0.9V _{DD}	---	-----	I _{OH} =-40uA	
Voltage Drop	V _{dCOM}	-----	---	1	IO=±0.1 mA	V
	V _{dSEG}	-----	---	1		
Input Leakage Current	I _{IL}	-1	---	1	V _{IN} =0 V to V _{DD}	uA
Input Low Current	I _{IN}	-50	-125	-250	V _{IN} =0V, V _{DD} =5V(pull up)	uA
Internal Clock (external Rf)	f _{IC}	190	270	350	Rf = 91k±2% (V _{DD} =5V)	kHz
External Clock	f _{EC}	150	250	350	----	kHz
	Duty	45	50	55	----	%
	t _R ,t _F	---	---	0.2	----	us
LCD Driving Voltage	V _{LCD}	4.6	---	10.0	V _{DD} -V5(1/5,1/4 Bias)	V

(CONTINUED)
(VDD=2.7V~4.5V, Ta=-20~+70°C)

Item	Symbol	Standard Value			Test Condition	Unit
		MIN	TYP	MAX		
Operating Voltage	V _{DD}	2.7	---	4.5	-----	V
Supply Current	I _{DD1}	----	0.3	0.5	Ceramic oscillation fosc=250kHz	mA
	I _{DD2}	----	0.17	0.3	Resistor oscillation external clock operation fosc=270kHz	
Input Voltage(1) (except OSC1)	V _{IL1}	-0.3	--	0.4	-----	V
	V _{IH1}	0.7V _{DD}	--	V _{DD}	-----	
Input Voltage(2) (OSC1)	V _{IL2}		--	0.2V _{DD}	-----	V
	V _{IH2}	0.7V _{DD}	--	V _{DD}	-----	
Output Voltage (1) (DB0 to DB7)	V _{OL1}	---	----	0.4	I _{OL} =0.1mA	V
	V _{OH1}	2.0	---	----	I _{OH} =-0.1mA	
Output Voltage (2) (except DB0 to DB7)	V _{OL2}	-----	---	0.2V _{DD}	I _{OL} =40uA	V
	V _{OH2}	0.8V _{DD}	---	-----	I _{OH} =-40uA	
Voltage Drop	V _{dCOM}	-----	---	1	IO=±0.1 mA	V
	V _{dSEG}	-----	---	1.5		
Input Leakage Current	I _{IL}	-1	---	1	V _{IN} =0 V to V _{DD}	uA
Input Low Current	I _{IN}	-10	-50	-120	V _{IN} =0V, V _{DD} =3V(pull up)	uA
Internal Clock (external Rf)	f _{IC}	190	250	350	Rf = 75k±2 % (V _{DD} =3V)	kHz
External Clock	f _{EC}	125	270	350	----	kHz
	Duty	45	50	55	----	%
	t _R , t _F	---	---	0.2	----	us
LCD Driving Voltage	V _{LCD}	3.0	---	10.0	V _{DD} -V5 (1/5, 1/4 Bias)	V

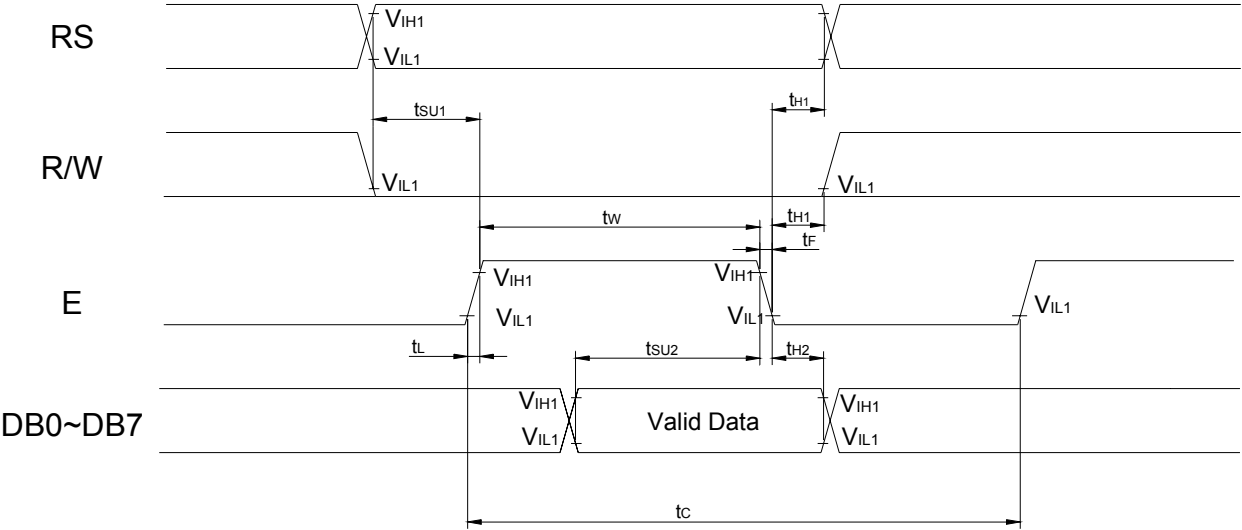
13-2 AC Characteristics**(V_{DD}=4.5V~5.5V, Ta=-20~+70°C)**

Mode	Item	Symbol	Min	Typ	Max	Unit
(1) Write Mode (refer to Figure 8.0)	E Cycle Time	t _C	500	---	---	ns
	E Rise/Fall Time	t _R , t _F	---	---	25	
	E Pulse Width (High, Low)	t _w	220	---	---	
	R/W and RS Setup Time	t _{su1}	40	---	---	
	R/W and RS Hold Time	t _{H1}	10	---	---	
	Data Setup Time	t _{su2}	60	---	---	
	Data Hold Time	t _{H2}	10	---	---	
(2) Read Mode (refer to Figure 9.0)	E Cycle Time	t _C	500	---	---	ns
	E Rise/Fall Time	t _R , t _F	---	---	25	
	E Pulse Width (High, Low)	t _w	220	---	---	
	R/W and RS Setup Time	t _{su}	40	---	---	
	R/W and RS Hold Time	t _H	10	---	---	
	Data Out Delay Time	t _D	---	---	120	
	Data Hold Time	t _{DH}	20	---	---	

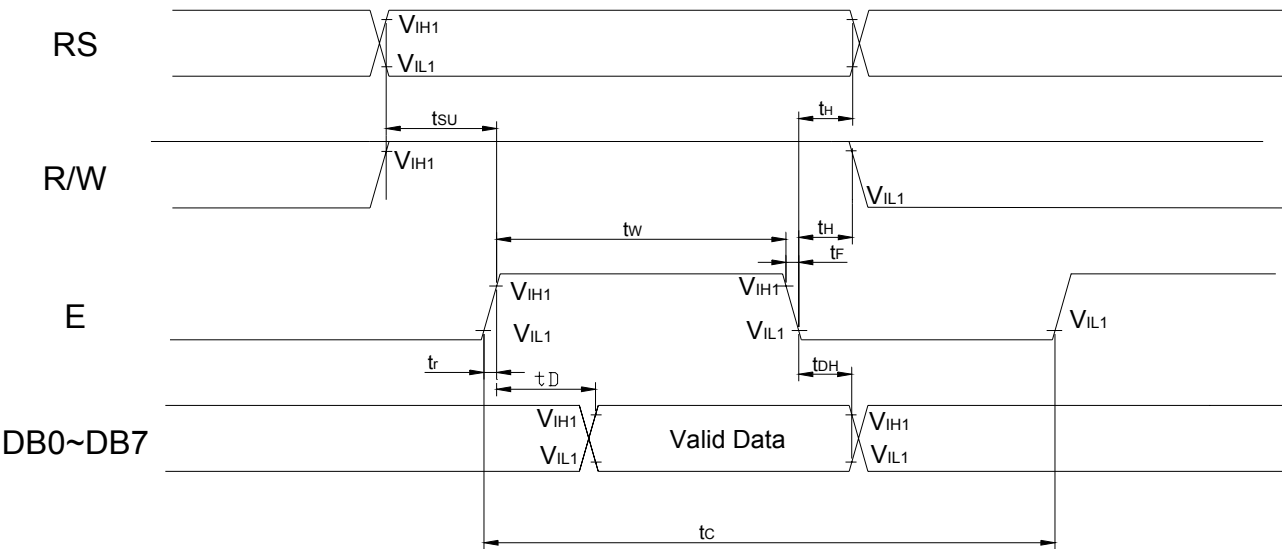
(V_{DD}=2.7V~4.5V, Ta=-20~+70°C)

Mode	Item	Symbol	Min	Typ	Max	Unit
(3) Write Mode (refer to Figure 8.0)	E Cycle Time	t _C	1400	---	---	ns
	E Rise/Fall Time	t _R , t _F	---	---	25	
	E Pulse Width (High, Low)	t _w	400	---	---	
	R/W and RS Setup Time	t _{su1}	60	---	---	
	R/W and RS Hold Time	t _{H1}	20	---	---	
	Data Setup Time	t _{su2}	140	---	---	
	Data Hold Time	t _{H2}	10	---	---	
(4) Read Mode (refer to Figure 9.0)	E Cycle Time	t _C	1400	---	---	ns
	E Rise/Fall Time	t _R , t _F	---	---	25	
	E Pulse Width (High, Low)	t _w	450	---	---	
	R/W and RS Setup Time	t _{su}	60	---	---	
	R/W and RS Hold Time	t _H	20	---	---	
	Data Out Delay Time	t _D	---	---	360	
	Data Hold Time	t _{DH}	5	---	---	

13-3-1 Write mode



13-3-2 Read mode



14. CHARACTER GENERATOR ROM (S6A0070)































































































































































































































Upper(4bit) Lower(4bit)	LLLL	LLHL	LLHH	LHLL	LHLH	LHHL	LHHH	HLLL	HLLH	HLHL	HLHH	HHLL	HHLH	HHHL	HHHH
LLLL	CG RAM (1)														
LLLH	(2)														
LLHL	(3)														
LLHH	(4)														
LHLL	(5)														
LHLH	(6)														
LHHL	(7)														
LHHH	(8)														
HLLL	(1)														
HLLH	(2)														
HLHL	(3)														
HLHH	(4)														
HHLL	(5)														
HHLH	(6)														
HHHL	(7)														
HHHH	(8)														

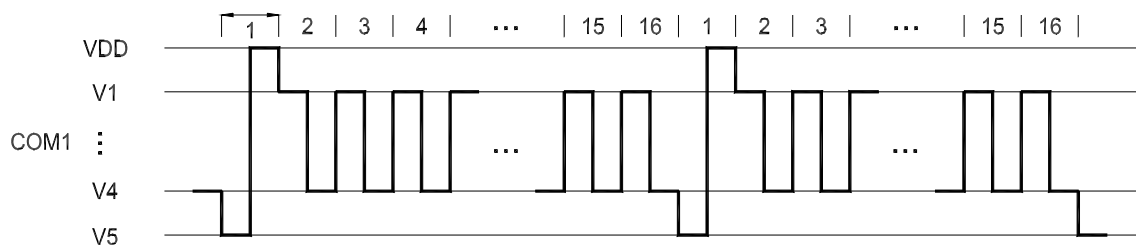
Table 3. Relationship Between character Code (DDRAM) and Character Pattern (CGRAM)

Character Code (DDRAM data)								CGRAM Address						CGRAM Data								Pattern number
D7	D6	D5	D4	D3	D2	D1	D0	A5	A4	A3	A2	A1	A0	P7	P6	P5	P4	P3	P2	P1	P0	
0	0	0	0	x	0	0	0	0	0	0	0	0	0	x	x	x	0					Pattern 1
											0	0	1					0	0	0		
											0	1	0					0	0	0		
											0	1	1									
											1	0	0					0	0	0		
											1	0	1					0	0	0		
											1	1	0					0	0	0		
											1	1	1				0	0	0	0	0	
0	0	0	0	x	1	1	1	1	1	1	0	0	0	x	x	x		0	0	0		Pattern 8
											0	0	1					0	0	0		
											0	1	0					0	0	0		
											0	1	1									
											1	0	0					0	0	0		
											1	0	1					0	0	0		
											1	1	0					0	0	0		
											1	1	1				0	0	0	0	0	

"x": don't care

15. FRAME FREQUENCY (1/16 duty cycle)

A-type Waveform



Item	Clock / Frequency
Line selection period	200 clocks
Frame frequency	84.4 Hz

* fosc = 270 kHz (1 clock = 3.7 us)

16. THE MODULE ACCEPT QUALITY LEVEL (AQL).

16.1 AQL Standard Value: Fatal Defect =0.1, Major Defect=0.65; Minor Defect =2.5.

16.2 Curtailed Inspection Scheme

Type	Batch Qty	inspection Qty	inspection rate	AQL value	pass	Reject
module product	350PCS< 1000PCS	125pcs	>25%	0.1	0	1
				0.65	2	3
				2.5	7	8
	200PCS< 350PCS	80pcs	>23%	0.1	0	1
				0.65	1	2
				2.5	5	6
	<200PCS	32pcs	>16%	0.1	0	1
				0.65	0	1
				2.5	4	5
Module sample	<200PCS	All inspected	/	/	/	The sample will be reject when the fateful defect>2pcs or main defect>5pcs.
	>200PCS	125pcs				

- Notes:** 1). Batch QTY is the production amount that Production department ship to QA department.
 2). All of product will be inspected if the batch QTY less than inspected QTY.
 3). Each batch fixed to be 500pcs.

17. RELIABILITY TEST

Operating life time: Longer than 50000 hours

(at room temperature without direct irradiation of sunlight)

Reliability characteristics shall meet following requirements.

TEMPERATURE TESTS	NORMAL GRADE
High temperature storage	+80℃ * 96hrs (Without Polarizer)
Low temperature storage	-30℃ * 4hrs
High temperature operation	+70℃ * 96hrs
Low temperature operation	-20℃ * 96hrs
High temperature, High humidity	+70℃ 95%RH 96hrs (Without Polarizer)
Thermal shock	-20℃ * 30 min 10s ↓ 5Cycles 70℃ * 30 min
Vibration test	Frequency * Swing * Time 40Hz * 4mm * 4hrs
Drop test	Drop height * Times 1.0m * 6 times

18. LCD MODULES HANDLING PRECAUTIONS

- Please remove the protection foil of polarizer before using.
- The display panel is made of glass. Do not subject it to a mechanical shock by dropping it from a high place, etc.
- If the display panel is damaged and the liquid crystal substance inside it leaks out, do not get any in your mouth. If the substance come into contact with your skin or clothes promptly wash it off using soap and water.
- Do not apply excessive force to the display surface or the adjoining areas since this may cause the color tone to vary.
- The polarizer covering the display surface of the LCD module is soft and easily scratched. Handle this polarize carefully.
- To prevent destruction of the elements by static electricity, be careful to maintain an optimum work environment.
 - Be sure to ground the body when handling the LCD module.
 - Tools required for assembly, such as soldering irons, must be properly grounded.
 - To reduce the amount of static electricity generated, do not conduct assembly and other work under dry conditions.
 - The LCD module is coated with a film to protect the display surface. Exercise care when peeling off this protective film since static electricity may be generated.
- Storage precautions
When storing the LCD modules, avoid exposure to direct sunlight or to the light of fluorescent lamps. Keep the modules in bags designed to prevent static electricity charging under low temperature / normal humidity conditions (avoid high temperature / high humidity and low temperatures below 0°C). Whenever possible, the LCD modules should be stored in the same conditions in which they were shipped from our company.

19. OTHERS

- Liquid crystals solidify at low temperature (below the storage temperature range) leading to defective orientation of liquid crystal or the generation of air bubbles (black or white). Air bubbles may also be generated if the module is subjected to a strong shock at a low temperature.
- If the LCD modules have been operating for a long time showing the same display patterns may remain on the screen as ghost images and a slight contrast irregularity may also appear. Abnormal operating status can be resumed to be normal condition by suspending use for some time. It should be noted that this phenomena does not adversely affect performance reliability.
- To minimize the performance degradation of the LCD modules resulting from caused by static electricity, etc. exercise care to avoid holding the following sections when handling the modules:
 - Exposed area of the printed circuit board
 - Terminal electrode sections