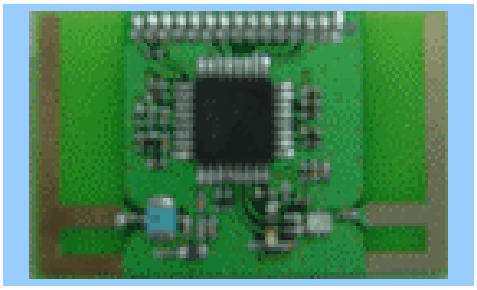
Holy Stone Enterprise Co., Ltd

MO-S724T-F2400

2.4GHz Transceiver MODULE



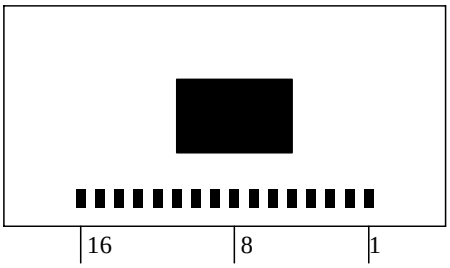
Description

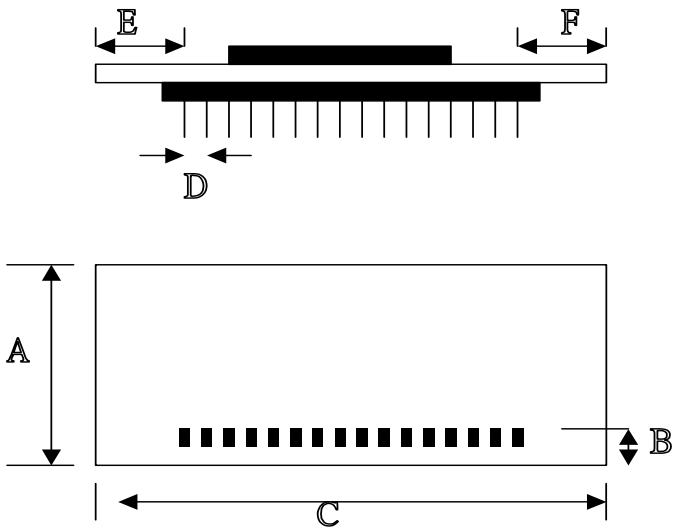
MO-S724T-F2400 is a 2.4GHz FSK Transceiver module. It is an entire Phase-Locked Loop (PLL) for precise local oscillator generation . It was use 3 wire mode to setting frequency and Function . It had a high performance and easily to design your product. .It can be used in wireless KB/Mouse and Wireless Game Pad system or specific remote-control function and others wireless system.

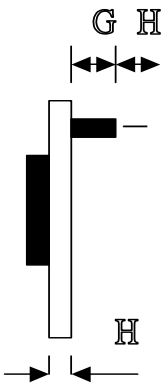
Applications

- Game Pad (PSX,PS1,PS2,XBOX…)
- PC control device
- Wireless mouse/Keyboard
- Automation system

(The received range about 10m)







Name	Dimension	Name	Dimension
A	22.3mm+-0.5mm	**E**	8.65mm
B	1.45mm+-0.3mm	**F**	9.1mm
C	36.8mm+-0.5mm	**G**	1mm
D	1.27mm	**H**	2.5mm

禾伸堂企業股份有限公司
Holy Stone Enterprise CO.,LTD

TEL:886-2-26596722
FAX:886-2-26596720
VER 2.0 2004-6-20

Absolute Maximum Ratings

Parameter	Rating	Units
Supply Voltage	4	V DC
Operating Temperature	-10~60	℃

Electric Characteristics (3.3V)

Parameter	Symbol	Condition	Specification			Unit
			Min.	Typical	Max.	
Operation Voltage	Vcc		2.7	3.3	3.8	V
Operation Current	Icc	Standby mode		10	100	uA
		Receiver	30	45	60	dBm
		Transmit	30	45	60	mA
Output Frequency	Fo	In 1.024MHz step	2.4028		2.4835	GHz
Transmit power	Po		-8	-5	-2	dBm
Receiver sensitivity		Data 250kBps	-	-75	-70	dBm
Data rate			20k	500k	1.5M	Bps
RSSI (figure3)	Vrssi max	-20dBm in	1.8	2.5		V
	Vrssi min	No signal	0.1			V
		mid range	28	35		MV/dBm
Time	To(tx-rx)	Tx to Rx time			120	us
	Tc(ch-ch)	Change CH		100		us
	Ts (sleep-Lo luck)	From XCEN PLL program		240	280	us
Reference Frequency	Fr		6.144	12.288		MHz

PIN CONFIGURATION

1	VCC	I	DC Power supply 2.7V~3.8V
2	REF	I	Input for 12.288MHz or 6.144 reference frequency
3	TPC/TPQ	O	Multi function output ,
4	PAON	O	External power amplifier control pin
5	EN	I	Enable pin for 3 wire control bus
6	CLK	I	Serial control bus data is clock for 3 wire control bus
7	DATA	I	Serial control bus data with 16 bits for 3 wire control bus
8	DOUT	O	Receiver serial digital output after demodulation.
9	DIN	I	Transmit data input
10	RSSI/TPI	O	Receiver signal strength indicaor
11	GND	O	GND
12	RXON	I	Receiver on
13	XCEN	I	Transceiver enable
14	VCC	I	DC Power supply 2.7V~3.8V
15	GND	O	GND
16	GND	O	GND

MODES OF OPERATION

There are three key modes of operation:

- **STANDBY:** All circuits powered down, except the control interface (Static CMOS)
- **RECEIVE:** Receiver circuits active
- **TRANSMIT:** Modulated RF output from IC

The two operational modes are RECEIVE and TRANSMIT, controlled by RXON. XCEN is the chip enable/disable control pin, which sets the part in operational or STANDBY modes. The relationship between the parallel control lines and the mode of operation of the IC is given in **Table 1**.

XCEN	RXON	MODE	FUNCTION
0	X	STANDBY	Control interfaces active, all other circuits powered down
1	1	RECEIVE	Receiver time slot
1	0	TRANSMIT	Transmit time slot

Table 1: Modes of Operation

Receive Signal Strength Indication (RSSI)

RSSI is an indication of field strength. It can be used to control transmit power to conserve battery life or it may be used to determine if a given channel is occupied. See Figure 3.

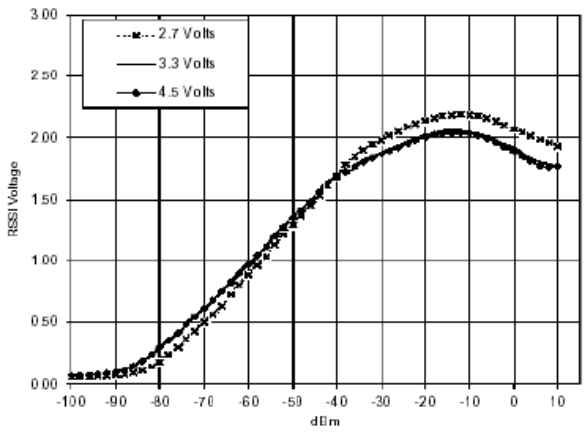


Figure 2. RSSI Output Voltage vs Input Signal Level
(Clipped, 25°C, Various Input Voltage Levels)

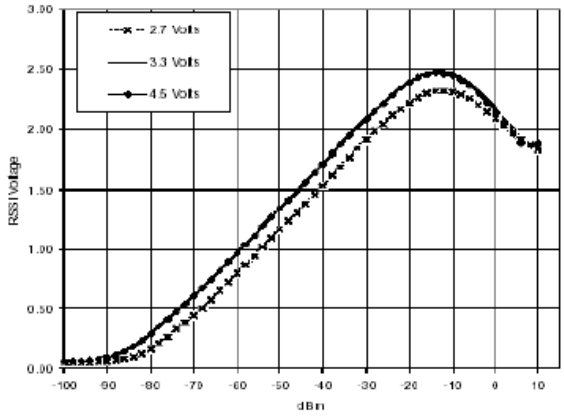


Figure 2a. RSSI Output Voltage vs Input Signal Level
(Unclipped, 25°C, Various Input Voltage Levels)

Figure 3: RSSI Voltage vs. Input Signal Level

SERIAL INTERFACE

A 3-wire serial interface (EN, DATA, CLK) is used for programming the ML2724 configuration registers, which control device mode, pin functions, PLL and reference dividers, internal test modes, and filter alignment. Data words are entered beginning with the MSB ("big-endian"). The word is divided into a leading 14-bit data field followed by a 2-bit address field. When the address field has been decoded the destination register is loaded on the rising edge of EN. **Providing less than 16 bits of data will result in unpredictable behavior when EN goes high.**

Data and clock signals are ignored when EN is high. When EN is low, data on the DATA pin is clocked into a shift register on the rising edge of the CLK pin. This information is loaded into the target control register when EN goes high. This serial interface bus is similar to that commonly found on PLL devices. It can be efficiently programmed by either byte or 16-bit word oriented serial bus hardware. The data latches are implemented in CMOS and use minimal power when the bus is inactive. Refer to Figure 4 and Table 2: 3-Wire Bus Timing Characteristics for timing and register programming illustrations.

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
BUS CLOCK (CLK)					
t_r	CLK input rise time			15	Ns
t_f	CLK input fall time			15	Ns
t_{ck}	CLK period	50			Ns
ENABLE (EN)					
t_{ew}	Minimum pulse width	100			Ns
t_l	Delay from last CLK rising edge	15			Ns
t_{se}	Set up time to ignore next rising CLK	15			Ns
BUS DATA (DATA)					
t_s	data to clock set up time	15			Ns
t_h	data to clock hold time	15			Ns

Table 2: 3-Wire Bus Timing Characteristics

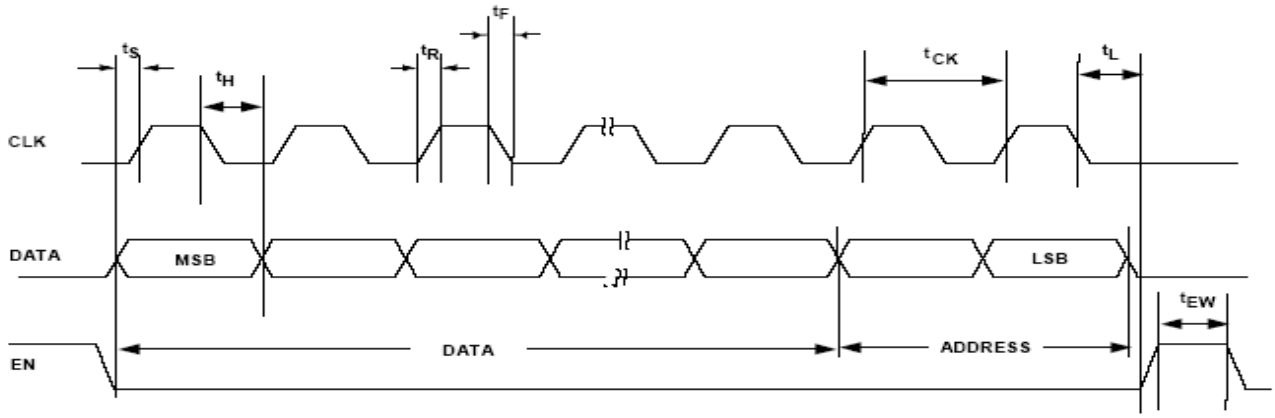


Figure 4: Serial Bus Timing for Address and Data Programming

CONTROL INTERFACES AND REGISTER DESCRIPTIONS

REGISTER INFORMATION

A 3-wire serial data input bus sets the ML2724's transceiver parameters and programs the PLL circuits. Entering 16-bit words into the ML2724 serial interface performs programming. Three 16-bit registers are partitioned such that 14 bits are dedicated for data to program the operation and two bits identify the register address. The contents of these registers cannot be read back via this bus.

The three registers are:

- **Register 0:** PLL Configuration
- **Register 1:** Channel Frequency Data
- **Register 2:** Internal Test Access

Figure 5 shows a register map. Table 3 through Table 5 provide detailed diagrams of the register organization: Table 3 and Table 4 outline the PLL configuration and channel frequency registers, and Table 5 displays the filter tuning and test mode register.

MSB

DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	ADR1	ADR0
Res.	Res.	Res.	Res.	RCLP	LVLO	Res.	TXM	TPC	TXCW	Res.	AOUT	RD0	QPP	0	0
B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0

MSB

DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	ADR1	ADR0
Res.	Res.	CHQ11	CHQ10	CHQ9	CHQ8	CHQ7	CHQ6	CHQ5	CHQ4	CHQ3	CHQ2	CHQ1	CHQ0	0	1
B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0

MSB

DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	ADR1	ADR0
Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	DTM2	DTM1	DTM0	ATM2	ATM1	ATM0	1	0
B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0

Figure 5: Configuration Register Map

NAME	DESCRIPTION	DEFINITION
Reserved	Reserved	Set all bits to 0 (zero)
Reserved	Reserved	
Reserved	Reserved	
Reserved	Reserved	
RCLP	RSSI Clip Disable	0: RSSI clipped to 1.9V at –15dBm 1: RSSI not clipped
LVLO	Low Voltage Lockout	0: PAON Undisturbed 1: PAON De-asserted for VCCA<2.65V. Reset on RXON high
Reserved	Reserved	Set to 0
TXM	TX RF Output Mode	0: TX RF Output always on in TX mode 1: TX RF Output follows PAON signal
TPC	Transmit Power Control	0: AOUT pin pulled to ground 1: AOUT pin high impedance
TXCW	Transmit Test Mode	0: FSK modulation in Transmit mode 1: CW (no modulation in Transmit mode)
Reserved	Reserved	Set to 0
AOUT	Analog Output	0: AOUT pin is Transmit Power Control 1: AOUT pin is Analog Data Out
RD0	Reference Frequency Select	0: 6.144MHz nominal reference frequency 1: 12.288MHz nominal reference frequency (preferred)
QPP	PLL Charge Pump Polarity	0: For fc < fref, charge pump sources current 1: For fc < fref, charge pump sinks current
ADR1	MSB Address Bit	ADR1=0
ADR0	LSB Address Bit	ADR0=0

Table 3: Register 0 -- PLL Configuration Register

NAME	DESCRIPTION	DEFINITION
Reserved	Channel Frequency select bits	Set all bits to 0 (zero)
Reserved		
CHQ11		Divide ratio=f_c/1.024
CHQ10		
CHQ9		
CHQ8		
CHQ7		
CHQ6		
CHQ5		
CHQ4		
CHQ3		
CHQ2		
CHQ1		
CHQ0		
ADR1	MSB Address Bit	ADR1=0
ADR0	LSB Address Bit	ADR0=1

Table 4: Register 1 – Channel Frequency Register

NAME	DESCRIPTION	DEFINITION
Reserved	Reserved	Set all bits to 0 (zero)
Reserved		
Reserved		
Reserved		
Reserved		
Reserved		
Reserved		
Reserved		
DTM2	Digital Test Control Bits	See Table 16
DTM1		
DTM0		
ATM2	Analog Test Control Bits	See Table 15
ATM 1		
ATM 0		
ADR1	MSB Address Bit	ADR1=0
ADR0	LSB Address Bit	ADR0=1

Table 5: Register 2 – Test Mode Register

CONTROL REGISTER BIT DESCRIPTIONS

ADR<1:0>, All Registers, Bits 0-1

Address Bits: The ADR<1:0> bits are the least-significant bits of each register. Each register is divided into a data field and an address field. The data field is the leading field, while the last two bits clocked into the register are always the address field. When EN goes high, the address field is decoded and the addressed destination register is loaded. The last 16 bits clocked into the serial bus are loaded into the register. Clocking in less than 16 bits results in a potentially incorrect entry into the register.

RES (Reserved), All Registers

Reserved Bits: These bits are reserved. These bits must be cleared to 0s (zeros) for normal operation. When power is reset, all of the registers' data fields are cleared to 0s (zeros).

QPP - Register 0, Bit 2

Charge Pump Polarity: This bit sets the charge pump polarity to sink or source current. For a majority of applications, this bit is cleared (QPP=0). For applications where an external inverting amplifier is used in the loop filter, this bit is set to change the charge pump polarity (see Table 6).

QPP	PLL CHARGE PUMP POLARITY
0	$f_c > f_{ref}$ =» Charge pump sinks current.
1	$f_c > f_{ref}$ =» Charge pump sources current.

Table 6: PLL Charge Pump Polarity

RD0 - Register 0, Bit 3

Reference Divide: This bit sets the reference divider from the FREF pin to the reference input of the PLL phase/frequency detector to either 9 or 18 (see Table 7).

RD0	REFERENCE DIVISION	FREF XTAL FREQ	PLL REF FREQ
0	9	6.144 MHz	682.67KHz
1	18	12.288 MHz	682.67KHz

Table 7: Reference Frequency Select

AOUT - Register 0, Bit 4

Analog Output Mode: This bit changes the function of the AOUT pin between an analog data output to transmit power control (see Table 8).

AOUT	AOUT PIN FUNCTION
0	Transmit Power Control
1	Data Filter Analog Output

Table 8: AOUT Function Select

TXCW - Register 0, Bit 6

Transmit Continuous Wave: This bit produces a continuous wave (CW) transmitter output for product test when RXON is low (see Table 9).

TXCW	TRANSMIT MODULATION
0	FSK Modulation
1	CW – No Modulation

Table 9: Transmit Modulation Mode

TPC - Register 0, Bit 7

Transmit Power Control: When the AOUT bit is low, this bit controls the state of the open-drain output pin. Although this bit can be changed at any time, the AOUT pin only changes state at the falling edge of RXON (see Table 10).

TPC	TPC PIN STATE
0	High Impedance
1	Pulled to Ground

Table 10: TPC Pin State

TXM - Register 0, Bit 8

Transmit Mode: This bit controls the TX RF buffer state timing mode. It must be reset to 0 for normal operation (see Table 11).

TXM	TXRF BUFFER BEHAVIOR
0	RF Output Always On in TX Mode
1	RF Output Follows PAON

Table 11: TXM Mode

LVLO - Register 0, Bit 10

Low Voltage Lock Out: The LVLO bit enables a transmit low voltage lockout latch, which shuts off the transmitter by de-asserting the PAON output. This latch is set if the supply voltage drops below 2.65V and is reset when the RXON control input goes high (see Table 12).

LVLO	PAON BEHAVIOR
0	PAON Undisturbed
1	PAON de-asserted when VCCA<2.65V, Reset by RXON high.

Table 12: LVLO Operation

RCLP - Register 0, Bit 11

RSSI Clip Enable: The RCLP bit disables the RSSI clipping circuitry. With RCLP low, the RSSI output voltage is clipped to a maximum of about 2.0V at –10dBm. With RCLP high, the RSSI is not clipped. (see Table 13).

RCLP	RSSI BEHAVIOR
0	RSSI output clipped to a maximum of ~1.9V at –15dBm
1	RSSI output not clipped

Table 13: RCLP Operation

CHQ <11:0> - Register 1, Bits 2-13

Channel Frequency Selection: These bits set the RF carrier frequency for the transceiver (see Table 14). With a 6.144MHz or 12.288MHz clock at the FREF pin, the channel frequency value is calculated by multiplying the CHQ value by 1.024. The recommended operating range value of the CHQ is from 2,346 to 2,424. These bits must be programmed to a valid channel frequency before XCEN is asserted.

B15	B14	B13 TO B2	B1	B0
0	0	CHQ - PLL Divide Ratio	0	1

Table 14: Main Divider

The divide ratio is calculated as f_c /1.024 where f_c is the channel frequency in MHz.

$$f_C = 1.024 * CHQ$$

ATM<2:0> - Register 2, Bits 2-4

Analog Test Mode: The test mode selected is described in Table 15. The performance of the ML2724 is not specified in these test modes. Although primarily intended for IC test and debug, they also can help in debugging the radio system. The default (power-up) state of these bits is ATM<2:0>=<0,0,0>. When a non-zero value is written to the field, the RSSI and AOUT pins become analog test access ports, giving access to the outputs of key signal processing stages in the transceiver. During normal operation, ATM<2:0> must be set to all zeros.

ATM2	ATM1	ATM0	RSSI	AOUT
0	0	0	RSSI	Set by AOUT bit
0	0	1	No Connect	No Connect
0	1	0	I IF Filter Output	Q IF Filter Output
0	1	1	Q IF Filter – ve Output	Q IF Filter + ve Output
1	0	0	I IF Filter – ve Output	I IF Filter + ve Output
1	0	1	Data Filter + ve Output	Data Filter – ve Output
1	1	0	I IF Limiter Outputs	Q IF Limiter Outputs
1	1	1	1.67V Voltage Reference	VCO Modulation Port Input

Table 15: Analog Test Control Bits

DTM <2:0> - Register 2, Bits 5-7

Digital Test Mode: The DTM<2:0> bit functions are described in Table 16. The performance of the ML2724 is not specified in these test modes. Although primarily intended for IC test and debug, they also can help in debugging the radio system. The default (power up) state of these bits is DTM<2:0>=<0,0,0>. When a non-zero value is written to these fields, the DOUT and PAON pins become a digital test access port for key digital signals in the transceiver. During normal operation, DTM<2:0> must be set to all zeros.

DTM2	DTM1	DTM0	PAON	DOUT
0	0	0	PA Control	Data Out
0	0	1	PA Control	AGC Switch State
0	1	0	PA Control	PLL Main Divider Output
0	1	1	PA Control	PLL Reference Divider Output
1	0	0	S – D Modulation LSB	Sigma – Delta Modulation MSB

Table 16: Digital Test Control Bits

PA CONTROL OUTPUTS (PAON & AOUT)

The PAON (PA control) is a CMOS output that controls an optional off-chip RF PA. It outputs a logic high when the PA should be enabled and a logic low at all other times. This output is inhibited when the PLL fails to lock.

AOUT (pin 7) normally supplies the analog (not data-sliced) data output, but it can also be configured as an open-drain output for transmit power control. This mode is controlled by the TPC bit in Register 0. This bit can be changed at any time, but the AOUT pin will not change mode until the beginning of the next transmit slot, triggered by a falling edge on RXON (see **Figure 6** and Table 17 for details).

In analog test modes the RSSI and AOUT pins become analog test access ports that allow the user to observe internal signals in the ML2724.

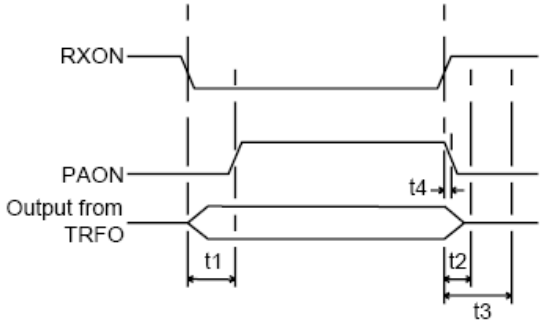


Figure 6: Power Amplifier Interface

SYMBOL	PARAMETER	TIME/µS
T1	RXON falling edge to PAON rising edge	62.5
T2	RXON rising edge to PLL frequency shift	6.5
T3	RXON rising edge to RECEIVE mode	70
T4	RXON rising edge to PAON falling edge	< 0.1

Table 17: Power Amplifier Timing