VLSI TECHNOLOGY, INC.

VL6522 • VL65C22 • VL65C22V

PARALLEL INTERFACE/TIMER

FEATURES

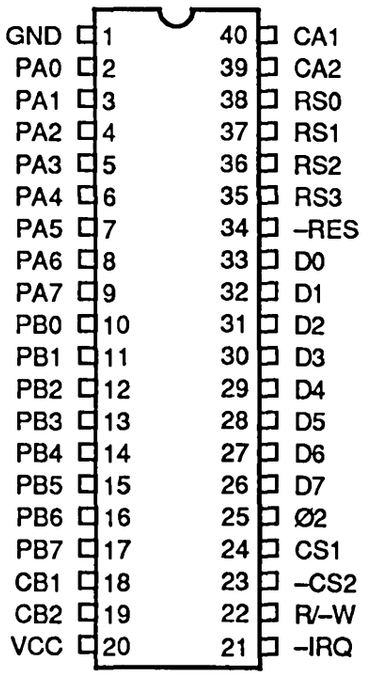
- Low power consuming CMOS parallel interface/timer
  - -VL65C22 has active pull-ups on Port "B"
  - -VL65C22V has resistive pull-ups on Port "B"
- Low cost HMOS parallel interface/timer (VL6522)
- Two 8-bit bidirectional I/O ports
- Two 16-bit timer/counters
- Serial bidirectional peripheral I/O port
- Programmable Data Direction Registers

DESCRIPTION

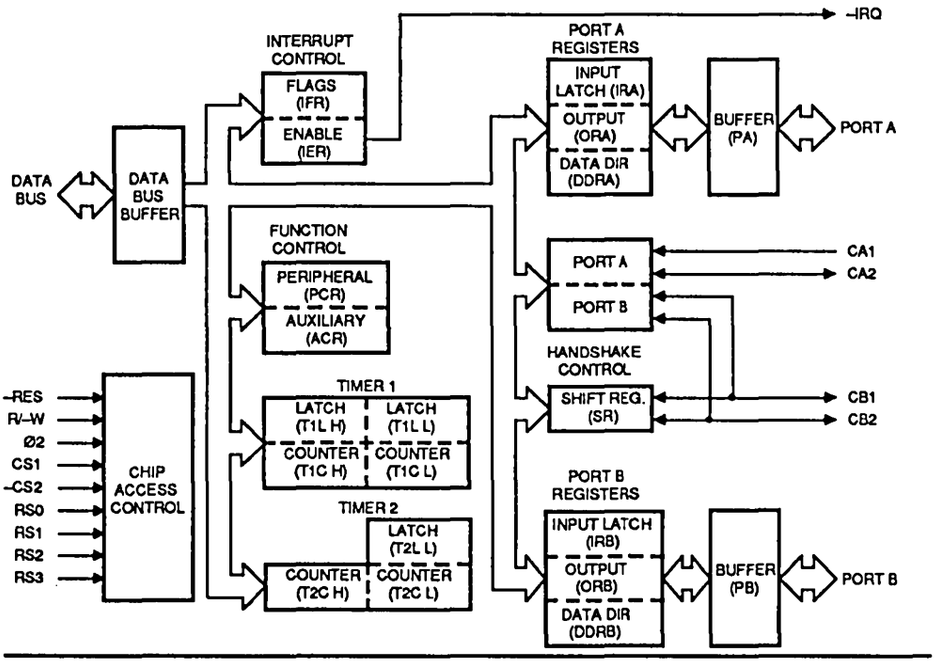
The VL6522/VL65C22/VL65C22V are flexible I/O devices for use with the 65XX family of processors. The VL65C22/VL65C22V are CMOS implementations of the VL6522 device. All include functions for programmed control of up to two peripheral devices (Ports A and B). Two program-controlled 8-bit bidirectional peripheral I/O ports allow direct interfacing between the microprocessor and selected peripheral devices. Two programmable Data Direction Registers (A and B) allow selection of data direction (input versus output) on an individual line-by-line basis. Also provided are two programmable 16-bit counter/timers with latches. Timer 1 may be operated in a one-shot interrupt mode with interrupts on each count-to-zero, or in a free-running mode with a series of evenly spaced interrupts. Timer 2 functions both as an interval and pulse counter. Serial data transfers are provided by a shift register. Application versatility is further increased by various control registers, including an interrupt flag register, an interrupt enable register, and two function control registers.

PIN DIAGRAM

VL6522
VL65C22
VL65C22V



BLOCK DIAGRAM



ORDER INFORMATION

Part Number	Technology	Clock Frequency	Package
VL6522-01PC	HMOS	1 MHz	Plastic DIP
VL6522-01QC	HMOS		Plastic Leaded Chip Carrier (PLCC)
VL6522-02PC	HMOS	2 MHz	Plastic DIP
VL65C22-02PC	CMOS		Plastic DIP
VL65C22V-02PC	CMOS		Plastic DIP
VL6522-02QC	HMOS		Plastic Leaded Chip Carrier (PLCC)
VL65C22-02QC	CMOS		Plastic Leaded Chip Carrier (PLCC)
VL65C22V-02QC	CMOS		Plastic Leaded Chip Carrier (PLCC)
VL65C22-04PC	CMOS	4 MHz	Plastic DIP
VL65C22V-04PC	CMOS		Plastic DIP
VL65C22-04QC	CMOS		Plastic Leaded Chip Carrier (PLCC)
VL65C22V-04QC	CMOS		Plastic Leaded Chip Carrier (PLCC)

Note: Operating temperature range is 0°C to +70°C

PIN DIAGRAM

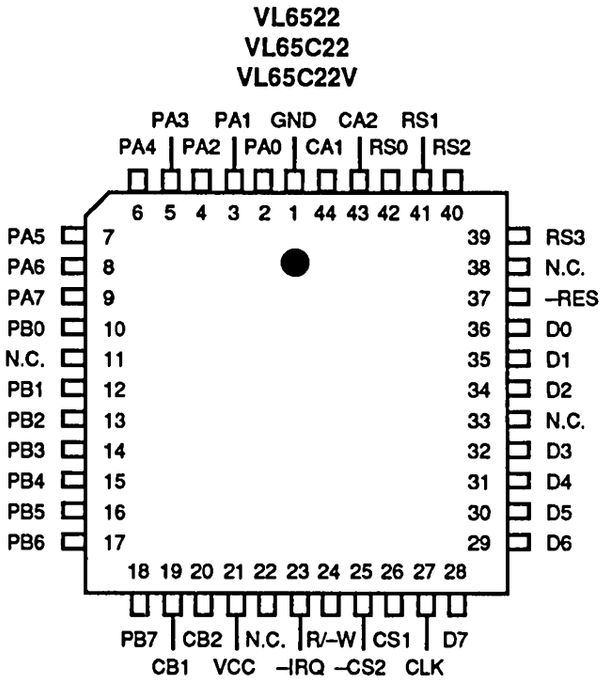
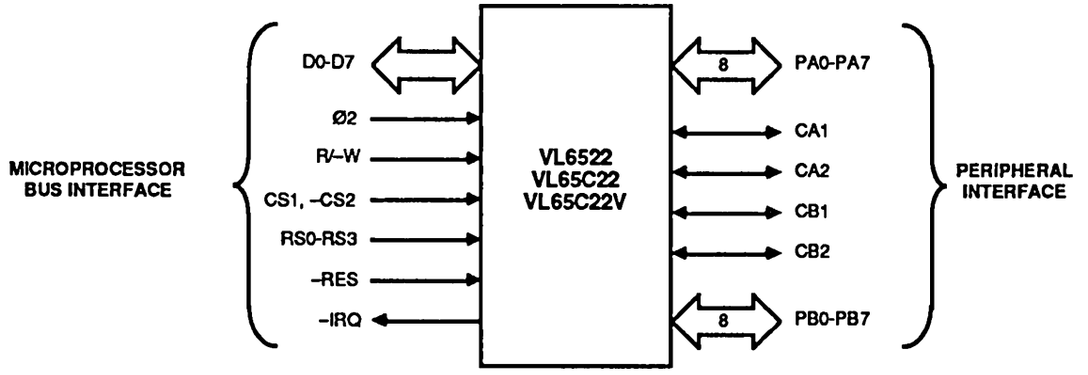


FIGURE 1. MICROPROCESSOR AND PERIPHERAL INTERFACE



FUNCTIONAL DIFFERENCES AMONG VL6522, VL65C22, AND VL65C22V

Function	VL6522	VL65C22	VL65C22V
Register Select Lines	Are Decoded During –Ø2	Are Decoded During –Ø2 Only if –CS2 is an Active Low	Are Decoded During –Ø2 Only if –CS2 is an Active Low
CB1	Must Not Change During Last 100 ns of –Ø2	Must Not Change During Last 100 ns of –Ø2	Can Change Anytime, But is Sampled Only During –Ø2
Port B (PB0 - PB7, CB1, CB2)	Has Active (Transistor) Internal Pull-ups	Has Active (Transistor) Internal Pull-ups	Has Passive (Resistor, Approx. 6 kohms) Internal Pull-ups
Port B (PB0 - PB7, CB1, CB2)	Each pin represents one Standard TTL load either as an input or as an output	Each pin represents two Standard TTL loads either as an input or as an output	Each pin represents one Standard TTL load either as an input or as an output

SIGNAL DESCRIPTIONS

Signal Name	Pin Number	Signal Description
–RES	34	AA low reset (–RES) input clears all VL65(C)22(V) internal registers to logic 0 (except T1 and T2 latches and counters and the Shift Register). This places all peripheral interface lines in the input state; disables the timers, shift register, and interrupting from the chip.
Ø2	25	The input clock is the system Ø2 clock and triggers all data transfers between processor bus and the VL65(C)22(V).
R/–W	22	The direction of the data transfers between the VL65(C)22(V) and the system processor is controlled by the R/–W line and the CS1 and –CS2 inputs. When R/–W is low, (write operation) and the VL65(C)22(V) is selected, data is transferred from the processor bus into the selected VL65(C)22(V) register. When R/–W is high, (read) and the chip is selected, and data is transferred from the selected VL65(C)22(V) register to the CPU.
D0-D7	33-26	The eight bidirectional data bus lines transfer data between the VL65(C)22(V) and the system processor bus. During ready cycles, the contents of the selected VL65(C)22(V) register are placed on the data bus lines. During write cycles, these lines are high-impedance inputs and data is transferred from the processor bus into the selected register. When the VL65(C)22(V) is not selected, the data bus lines are high-impedance.
CS1, –CS2	24, 23	The two chip select inputs are normally connected to processor address lines either directly or through decoding. The selected VL65(C)22(V) register is accessed when CS1 is high and –CS2 is low.
RS0, RS1, RS2, RS3	38 - 35	The coding of the four Register Select inputs selects one of the 16 internal registers of the VL65(C)22(V), as shown in Table 2.
–IRQ	21	The Interrupt Request output goes low whenever an internal interrupt flag is set and the corresponding interrupt enable bit is a logic 1. This output is open-drain to allow the interrupt request signal to be wire-or'd with other equivalent signals in the system.
PA0 - PA7	2 - 9	Port A consists of eight lines which can be individually programmed to act as inputs or outputs under control of Data Direction Register A. The polarity of output pins is controlled by an Output Register and input data may be latched into an internal register under control of CA1 line. All modes of operation are controlled by the system processor through the internal control registers. These lines, as inputs represent one standard TTL load in the input mode and will drive one standard TTL load in the output mode.
PB0 - PB7	10 - 17	Peripheral Data Port B is an 8-line, bidirectional bus, controlled by an Output Register, Input Register and Data Direction Register similar to Data Port A. The output signal on line PB7 may be controlled by Timer 1 while Timer 2 may be programmed to count pulses on PB6 line. VL6522 and VL65C22 Port B lines are also capable of sourcing 3.0 mA at 1.5 VDC in the output mode. This allows the outputs to directly drive Darlington transistor circuits. VL65C22V Port B lines have internal pull-up resistors (3 kΩ) to VCC.
CA1, CA2	40, 39	Control Lines CA1 and CA2 serve as interrupt inputs or handshake outputs for Peripheral Data Port A. Each line controls an internal Interrupt Flag with a corresponding Interrupt Enable bit. CA1 also controls the latching of Input Data on Port A. CA1 is a high impedance input, while CA2 represents one standard TTL load in the input mode. In the output mode, CA2 will drive one standard TTL load.
CB1, CB2	18, 19	Control lines CB1 and CB2 are interrupt inputs or handshake outputs for Peripheral Data Port B. Like Port A, these two lines control an internal Interrupt Flag with a corresponding Interrupt Enable bit. These lines are also a serial data port under control of the Shift Register (SR). Each control line represents two standard TTL loads in the input mode (one TTL load on the VL65C22V) and can drive two TTL loads in the output mode (one TTL load for the VL65C22V). CB1 and CB2 cannot drive Darlington transistor circuits.
VCC	20	+5 Volts
GND	1	Ground

FUNCTIONAL DESCRIPTION

PERIPHERAL DATA PORTS (PORT A, PORT B)

Each Peripheral Data Port operates in conjunction with a Data Direction Register (DDRA or DDRB). Under program control, the Data Direction Registers specify which lines within the port bus are to be designated as inputs or outputs. A Logic 0 in any bit position of the register will cause the corresponding line to serve as an input, while a Logic 1 will cause the line to serve as an output.

When a line is programmed as an output, it is controlled by a corresponding bit in the Output Register (ORA or ORB). A Logic 1 in the Output Register will cause the corresponding output line to go high, while a Logic 0 will cause the line to go low. Under program control, data is written into the Output Register bit positions corresponding to the output lines which have been programmed as outputs. Should data be written into bit positions corresponding to lines which have been programmed as inputs, the output lines will be unaffected.

When reading a Peripheral Data Port, the contents of the corresponding Input Register (IRA or IRB) are transferred onto the Data Bus. When the input latching feature is disabled, Input Register A (IRA) will reflect the logic levels present on the Port A bus lines. However, with input latching enabled and the selected active transition on CA1 having occurred, Input Register A will contain the data present on the Port A bus lines at the time of the transition. In this case, once Input Register A has been read, it will appear transparent, reflecting the current state of the Port A bus lines until the next CA1 latching transition.

With respect to Input Register B, it operates similar to Input Register A except that for those Port B bus lines which have been programmed as outputs, there is a difference. When reading Input Register A, the logic level on the bus line determines whether a Logic 1 or 0 is sensed. However, when reading the Input Register B, the logic level stored in Output Register B (ORB) is the logic level sensed. For this reason, those outputs which have large loading effects may cause the reading of Input Register A to result in the reading of Logic 0 when a 1 was actually programmed, and reading a Logic 1 when a 0 was programmed. However, when reading Input Register B, the logic level read will be correct, regardless of loading on the particular bus line.

For information on formats and operation of the Peripheral Data Port registers, refer to Figures 14, 15, 16, and 17. It should be noted that the input latching modes are controlled by the Auxiliary Control Register .

DATA TRANSFER - HANDSHAKE CONTROL

A powerful feature of the VL65(C)22(V) is its ability to provide absolute control over data transfers between the microprocessor and peripheral devices. This control is accomplished by way of "handshake" lines. Port A lines (CA1, CA2) handshake data transfers on both Read and Write operations, while Port B lines (CB1, CB2) handshake data on Write operations only.

READ HANDSHAKE CONTROL

Read Handshaking provides effective control of data transfers from a peripheral device to the microprocessor. To accomplish the Read Handshake, the peripheral device generates a Data Ready signal to the VL65(C)22(V) which indicates valid data is present on the Peripheral Data Port bus. In most cases, this Data Ready signal will interrupt the microprocessor, which will then read the data and generate a Data Taken signal. Once the peripheral senses the Data Taken signal, new data will be placed on the bus. This process continues until the data transfer is complete.

Automatic Read Handshaking applies to Peripheral Data Port A only. The Data Ready signal is transmitted by the peripheral device over the CA1 interrupt line, while the Data Taken signal is generated and transmitted to the peripheral device over the CA2 line. When the Data Ready signal is received, it sets an internal flag in the Interrupt Flag Register (IFR). This flag may interrupt the microprocessor or it may be polled under program control. As an option, the Data Taken signal may be either a pulse or a level. In either case, it is set low (Logic 0) by the microprocessor and is cleared by the next Data Ready signal. Refer to Figures 2 and 3 for Read Handshake timing and operating sequence.

WRITE HANDSHAKE CONTROL

The Write Handshake operation is similar to Read Handshaking. For Write Handshaking, however, the VL65(C)22(V) generates the Data Ready signal and the peripheral device must generate the Data Taken return signal. Note that Write Handshaking may occur on both Data Ports (A and B). For a Write Handshake, CA2 or CB2 serve as the Data Ready output and can operate in either the Handshake Mode or the Pulse Mode. The Data Taken signal is received by CA1 or CB1. The Data Taken signal sets a flag in the Interrupt Flag Register and clears the Data Ready output signal. Note that the selection of Read or Write Handshake operating modes (CA1, CA2, CB1, and CB2) is accomplished by the Peripheral Control Register (PCR).

INTERRUPT OPERATION

There are three basic operations, including: setting the flag within the Interrupt Flag Register (IFR), enabling the interrupt by way of a corresponding bit in the Interrupt Enable Register (IER), and signaling the microprocessor with an Interrupt Request (IRQ). An Interrupt Flag can be set by conditions Internal to the chip or by inputs to the chip from external sources. Normally, an Interrupt Flag remains set until the interrupt is serviced. To determine the source of an interrupt, the microprocessor must examine each flag in order, from highest to lowest priority. This is accomplished by reading the contents of the Interrupt Flag Register into the microprocessor accumulator, shifting the contents either left or right and then using conditional branch instructions to detect an active interrupt. Each Interrupt Flag has a corresponding Interrupt Enable bit in the Interrupt Enable Register. The enable bits are controlled by the microprocessor (set or reset). If an Interrupt Flag is high (Logic 1), and the corresponding Interrupt Enable bit is high (Logic 1), the Interrupt Request (IRQ) will go low (Logic 0).

FUNCTIONAL DESCRIPTION (Cont.)

IRQ is an open-collector output which can be wire-or'd with other devices within the system.

All Interrupt Flags are contained within a single Interrupt Flag Register. Bit 7 of this register will be high (Logic 1) whenever an Interrupt Flag is set, thus allowing convenient polling of several devices within a system to determine the source of the interrupt.

The Interrupt Flag Register (IFR) and Interrupt Enable Register (IER) format and operation is shown in Figures 28 and 29 respectively. The Interrupt Flag Register may be read directly by the micrprocessor, and individual flag bits may be cleared by Writing a "1" into the appropriate bit of the IFR. Bit 7 of the IFR indicates the status of the Interrupt Request (IRQ) output. Bit 7 corresponds to the following logic function: IRQ = IFR6 x IER6 + IFR5 x IER5 + IFR4 x IER4 + IFR3 x IER3 + IFR2 x IER2 + IFR1 x IER1 + IFR0 x IER0. Note x = LogicAND, + = LogicOR.

Bit 7 is not a flag. For this reason, bit 7 is not directly cleared by writing a "1" into its bit position. It can be cleared, however, by clearing all the flags within the register, or by disabling all active interrupts in the next section.

TIMER OPERATION

Timer 1 Operation - Interval Timer T1 consists of two 8-bit latches and a 16-bit counter. The latches serve to store data which is to be loaded into the counter. Once the counter is loaded under program control, it decrements at a Phase 2 (Ø2) clock rate. Upon reaching zero, an Interrupt Flag is set, causing Interrupt Request (IRQ) to go low (Logic 0) if the corresponding Interrupt Enable bit is set. Once the Timer reaches a count of zero, it will either disable any further interrupts (provided it has been programmed to do so), or it will automatically transfer the contents of the latches into the counter and proceed to decrement again. The counter may be programmed to invert the output signal on PB7 each time it reaches a count of zero. Additional control bits are provided in the Auxiliary Control Register (bits 6 and 7) to allow selection of Timer 1 operating modes.

It should be noted that the microprocessor does not write directly into the low-order counter (T1C-L). Instead, this half of the counter is loaded automatically from the low-order register when the microprocessor writes into the high-order register and counter. In fact, it may not be necessary to write to the low-order register in some applications since the timing operation is triggered by writing to the high-order register and counter.

Timer 1 One-Shot Mode - Interval Timer T1 may operate in the One-Shot Mode which allows the generation of a single Interrupt Flag each time the Timer is loaded. The Timer can also be programmed to produce a single negative pulse on Data Port Line PB7.

To generate a single interrupt, it is required that bits 6 and 7 of the Auxiliary Control Register be low (Logic 0). The low-order T1 counter (T1C-L) or the low-order T1 latch (T1L-L) must then be loaded with the low-order count value. Note that a load to T1C-L is effectively a load to T1L-L. Next, the high-order count value must be loaded into the high-order T1 counter (T1C-H), at which time the value is simultaneously loaded into high-order T1 latch (T1L-H). During this load sequence, the contents of T1L-L is transferred to T1C-L. The counter will start counting down on the next Ø2 clock following the load sequence into T1C-H, and will decrement at the Ø2 clock rate. Once the T1 counter reaches a zero count, the Interrupt Flag is set. To generate a negative pulse on Data Port line PB7, the sequence is identical to the above except bit 7 of the Auxiliary Control Register must be high (Logic 1). Data Port line PB7 will then go low (Logic 0) following the load to T1C-H, and will go high (Logic 1) again when the counter reaches a zero count. Once set, the T1 Interrupt Flag is reset by either loading T1C-H, which starts a new count, or by reading T1C-L.

Timer 1 Free-Run Mode - An important advantage within the VL65C22 is the ability of the latches associated with the T1 counter to provide a continuous series of evenly spaced interrupts or a square wave on Data Port line PB7. It should also be noted that the continuous series of interrupts and square waves are not affected by variations in the microprocessor interrupt response time. These advantages are all produced in the Free-Run Mode. When operating in the Free-Run Mode, the Interrupt Flag is set and the signal on PB7 is inverted each time the counter reaches a count of zero. In the Free-Run Mode, however, the counter does not continue to decrement after reaching a zero count. Instead, the counter automatically transfers the contents of the latch into the counter (16 bits) and then decrements from the new count value. As can be seen, it is not necessary to reload the timer in order to set the Interrupt Flag on the next count of zero. When set, the Interrupt Flag can be cleared by either reading T1C-L, by writing directly into the Interrupt Flg Register (IFR) as will be discussed later, or by a load into T1C-H when a new count value is desired.

Since the interval timers are all retriggerable, reloading the counter will always reinitialize the time-out period. Should the microprocessor continue to reload the counter before it reaches zero, counter time-out can be prevented. Timer 1 is able to operate in this manner provided the microprocessor writes into the high-order counter (T1C-H). By loading the latches only, the microprocessor can access the timer during each count-down operation without affecting the time-out in progress. In this way, data loaded into the latches will determine the length of the next subsequent time-out period. This capability is of value in the Free-Run Mode with the output enabled. In the Free-Run Mode, the signal on Data Port line PB7 is inverted and the Interrupt Flag is set with each counter time-out. When the microprocessor responds to the interrupts with new data for the latches, it can determine the period of the next half-cycle during each half-cycle of the output signal on line PB7. In this way, complex waveforms can be generated.

Timer 2 Operation - Timer 2 operates in the One-Shot Mode only (as an interval timer), or as a pulse counter for

FUNCTIONAL DESCRIPTION (Cont.)

counting negative pulses on Data Port line PB6. A single control bit within the Auxiliary Control Register is used to select between these two modes. Timer 2 is made up of a write-only low-order latch (T2L-L), a read-only low-order counter (T2C-L), and a read/write high-order counter (T2C-H). This 16-bit counter decrements at a Ø2 clock rate.

Timer 2 One-Shot Mode - Operation of Timer 2 in the One-Shot Mode is similar to Timer 1. That is, for each load T2C-H operation, Timer 2 sets the Interrupt Flag for each countdown to zero. However, after a time-out, the T2 counters roll over to all 1's (FFF16) and continue to decrement. This two's complement decrement allows the user to determine how long the T2 Interrupt Flag has been set. Since the Interrupt Flag logic is disabled after the initial interrupt set (zero count), further interrupts cannot be set by a subsequent count to zero. To enable the Interrupt Flag logic, the microprocessor must reload T2C-H. The Interrupt Flag is cleared by either reading T2C-L or by loading T2C-H.

Timer 2 Pulse Counting Mode-In the Pulse Counting Mode, Timer 2 counts a predetermined number of negative-going pulses on Data Port line PB6. To accomplish this, a count number is loaded into T2C-H, which clears the Interrupt Flag logic and starts the counter to decrement each time a negative pulse is applied to Data Port line PB6. When the T2 counter reaches a count of zero, the Interrupt Flag is set and the counter continues to decrement with each pulse on PB6. To enable the Interrupt Flag for subsequent countdowns, it is necessary to reload T2C-H. The decrement pulse on line PB6 must be low (Logic 0) during the leading edge of the Ø2 clock.

SHIFT REGISTER OPERATION AND MODES

Shift Register Operation - The Shift Register performs bidirectional serial data transfers on line CB2. These transfers are controlled by an internal modulo-8 counter. Shift pulses can be applied to the CB1 line for controlling external devices. Each Shift Register operating mode is controlled by control bits within the Auxiliary Control Register.

Shift Register Input Modes - Shift Register Disabled (000) - In the 000 mode, the Shift Register is disabled from all operation. the microprocessor can read or write the Shift Register, but shifting is disabled and both CB1 and CB2 are controlled by bits in the Peripheral Control Register (PCR). The Shift Register Interrupt Flag is held low (disabled).

Shift In - Counter T2 Control (001) - In this mode, the shifting rate is controlled by the low order eight bits of counter T2. Shift pulses are generated on the CB1 line to control shifting in external devices. The time between transitions of the CB1 output clock is determined by the Ø2 clock period and the contents of the low-order T2 latch (N). Shifting occurs by writing or reading the Shift Register. Data is shifted into the low-order bit first, and is then shifted into the next higher order bit on the negative-going edge of each clock pulse. Input data should change before the positive-going edge of the CB1 clock pulse. This data is then shifted into the Shift Register during the Ø2 clock cycle following the positive-going edge of the CB1 clock pulse. After eight CB1 clock pulses, the Shift Register Interrupt Flag will set the IRQ will go low (Logic 0).

Shift In - Ø2 Clock Control (010) - In this mode, the shift rate is controlled by the Ø2 clock frequency. Shift pulses are generated on the CB1 line to control shifting in external devices. Timer 2 operates as an independent interval timer and has no influence on the Shift Register. Shifting occurs by reading or writing the Shift Register. Data is shifted into the low order bit first, and is then shifted into the next higher order bit on the trailing edge of the Ø2 clock pulse. After eight clock pulses, the Shift Register Interrupt Flag will be set and output clock pulses on the CB1 line will stop.

Shift In - External CB1 Clock Control (011) - In this mode, CB1 serves as an input to the Shift Register. In this way, an external device can load the Shift Register at its own pace. The Shift Register counter will interrupt the microprocessor after each eight bits have been shifted in. The Shift Register counter does not stop the shifting operation. Its function is simply that of a pulse counter. Reading or writing the Shift Register resets the Interrupt Flag and initializes the counter to count another eight pulses. Note that data is shifted during the first Ø2 clock cycle following the positive-going edge of the CB1 shift pulse. For this reason, data must be held stable during the first full cycle following CB1 going high.

Shift Out - Free Running at T2 Rate (100) -This mode is similar to mode 101 in which the shifting rate is determined by T2. However, in mode 100 the Shift Register Counter does not stop the shifting operation. Since Shift Register bit 7 (SR7) is recirculated back into bit 0, the eight bits loaded into the Shift Register will be clocked onto the CR2 line repetitively. In this mode, the Shift Register Counter is disabled and IRQ is never set.

Shift Out - T2 Control (101) - In this mode, the shift rate is controlled by T2 (as in mode 100). However, with each read or write of the Shift Register, the Shift Register Counter is reset and eight bits are shifted onto the CB2 line. At the same time, eight shift pulses are placed on the CB1 line to control shifting in external devices. After the eight shift pulses, the shifting is disabled, the Interrupt Flag is set, and CB2 will remain at the last data level.

Shift Out - Ø2 Clock Control (110) - In this mode, the shift rate is controlled by the system Ø2 Clock.

Shift Out - External CB1 Clock Control (111) - In this mode, shifting is controlled by external pulses applied to the CB1 line. The Shift Register Counter sets the Interrupt Flag for each eight-pulse count, but does not disable the shifting function. Each time the microprocessor reads or writes to the Shift Register, the Interrupt Flag is reset and the counter is initialized to begin counting the next eight pulses on the CB1 line. After eight shift pulses, the Interrupt Flag is set. The microprocessor can then load the Shift Register with the next eight bits of data.

TABLE 1. PERIPHERAL INTERFACE CHARACTERISTICS TA = 0°C to 70°C, VCC = 5 V ±5%

Symbol	Parameter	Min	Typ	Max	Unit
tR, tF	Rise and Fall Time for CA1, CB1, CA2 and CB2 Input Signals			1.0	µs
tCA2	Delay Time, Clock Negative Transition to CA2 Negative Transition (Read Handshake or Pulse Mode)			1.0	µs
tRS1	Delay Time, Clock Negative Transition to CA2 Positive Transition (Pulse Mode)			1.0	µs
tRS2	Delay Time, CA1 Active Transition to CA2 Positive Transition (Handshake Mode)			2.0	µs
tWHS	Delay Time, Clock Positive Transition to CA2 or CB2 Negative Transition (Write Handshake)	0.05		1.0	µs
tDS	Delay Time, Peripheral Data Valid to CB2 Negative Transition	0.20		1.5	µs
tRS3	Delay Time, Clock Positive Transition to CA2 or CB2 Positive Transition (Pulse Mode)			1.0	µs
tRS4	Delay Time, CA1 or CB1 Active Transition to CA2 or CB2 Positive Transition (Handshake Mode)			2.0	µs
t21	Delay Time Required from CA2 Output to CA1 Active Transition (Handshake Mode)	400			ns
tIL	Set-up Time, Peripheral Data Valid to CA1 or CB1 Active Transition (Input Latching)	300			ns
tSR1	Shift-Out Delay Time - Time from Ø2 Falling Edge to CB2 Data Out			300	ns
tSR2	Shift-In Set-up Time - Time from CB2 Data In to Ø2 Rising Edge	300*			ns
tSR3	External Shift Clock (CB1) Set-up Time Relative to Ø2 Trailing Edge	100		tCYC	ns
tIPW	Pulse Width - PB6 Input Pulse	2 x tCYC			
tICW	Pulse Width - CB1 Input Clock	2 x tCYC			
tIPS	Pulse Spacing - PB6 Input Pulse	2 x tCYC			
tICS	Pulse Spacing - CB1 Input Pulse	2 x tCYC			
tAL	CA1, CB1 Set Up Prior to Transition to Arm Latch	300			ns
tPDH	Peripheral Data Hold After CA1, CB1 Transition	150			ns

***Note:** This specification is "0" (zero) on the VL65C22V.

FIGURE 2. TIMING FOR READ HANDSHAKE, PULSE MODE

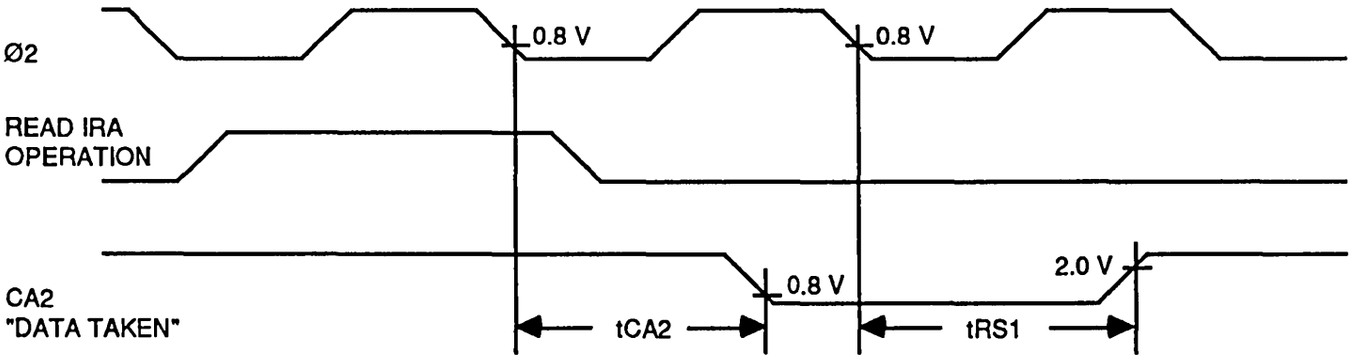


FIGURE 3. TIMING FOR READ HANDSHAKE, HANDSHAKE MODE

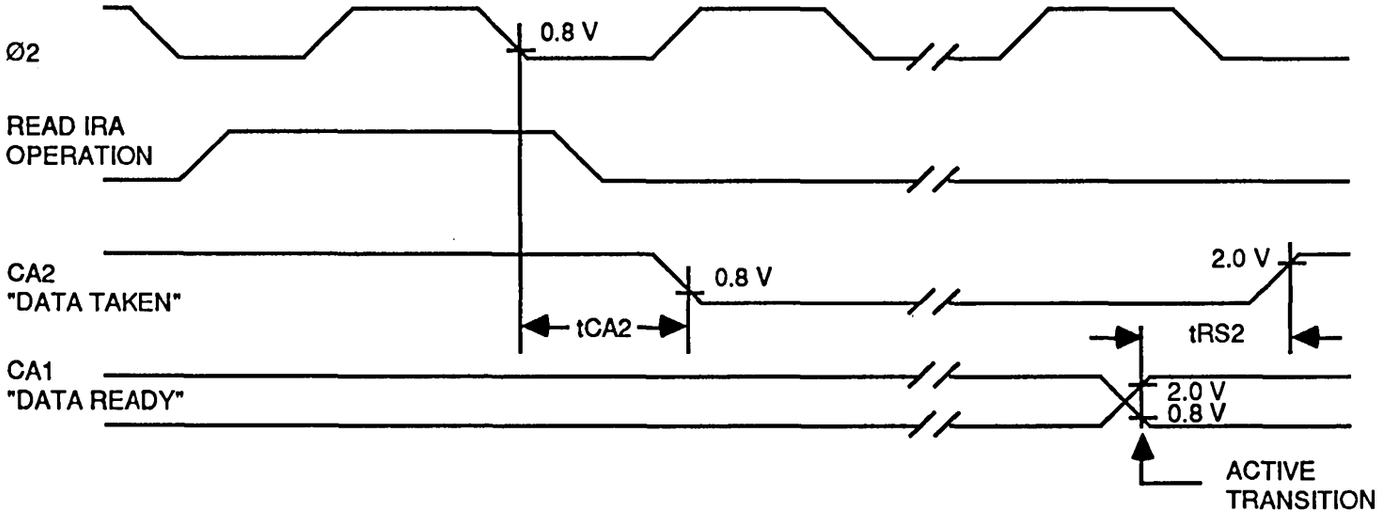


FIGURE 4. TIMING FOR WRITE HANDSHAKE, PULSE MODE

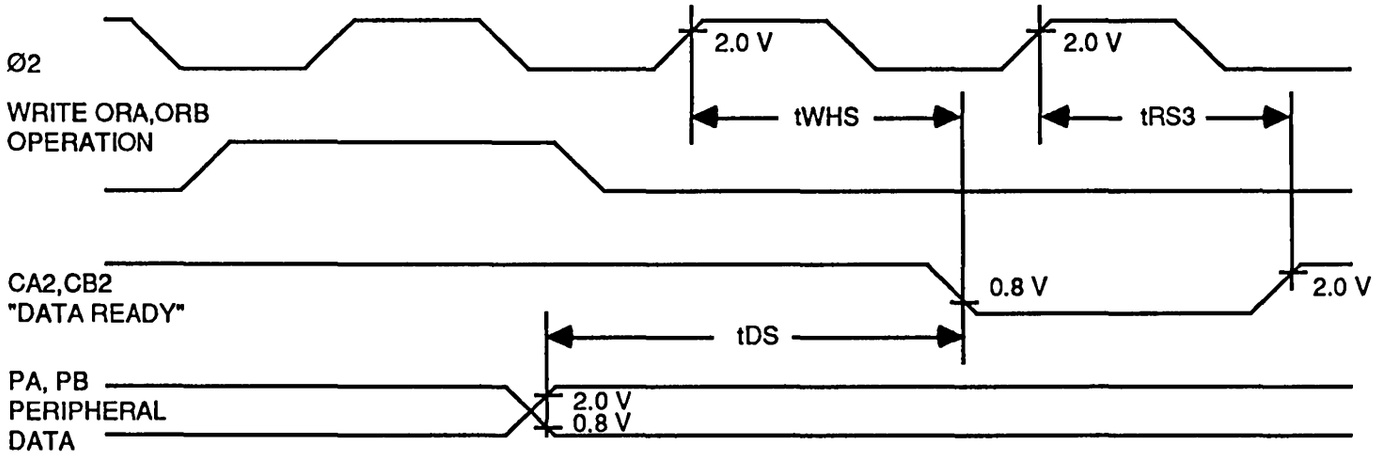


FIGURE 5. TIMING FOR WRITE HANDSHAKE, HANDSHAKE MODE

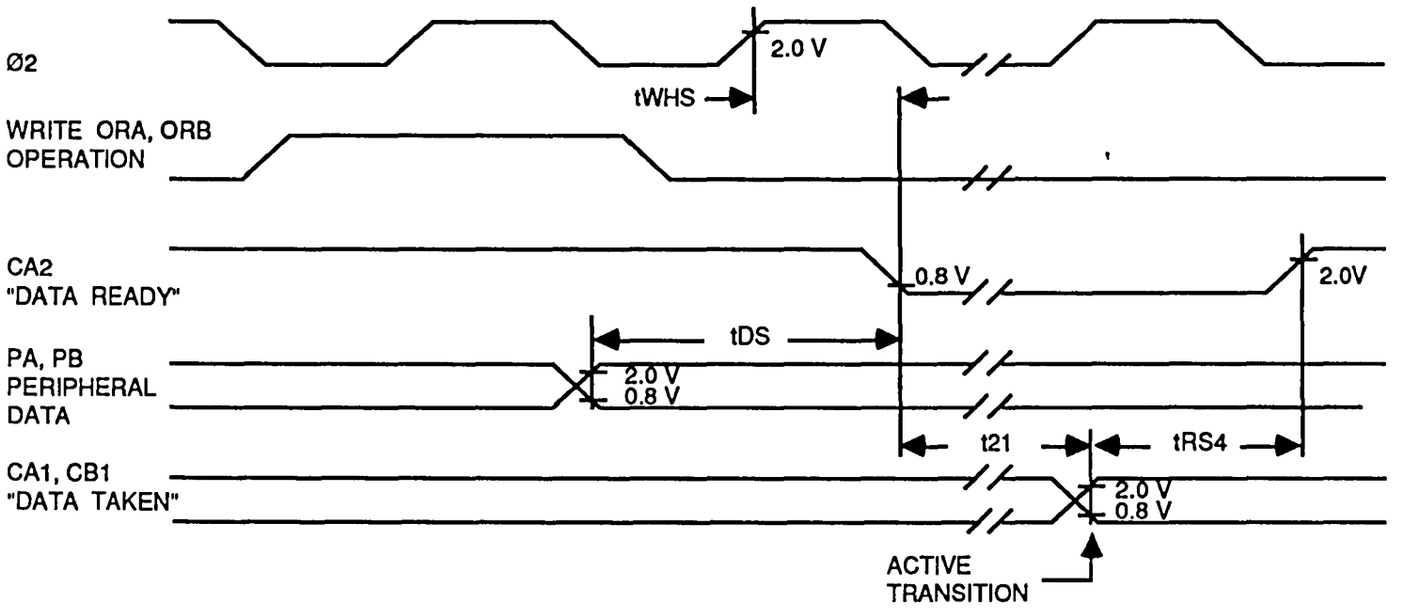


FIGURE 6. PERIPHERAL DATA INPUT LATCHING TIMING

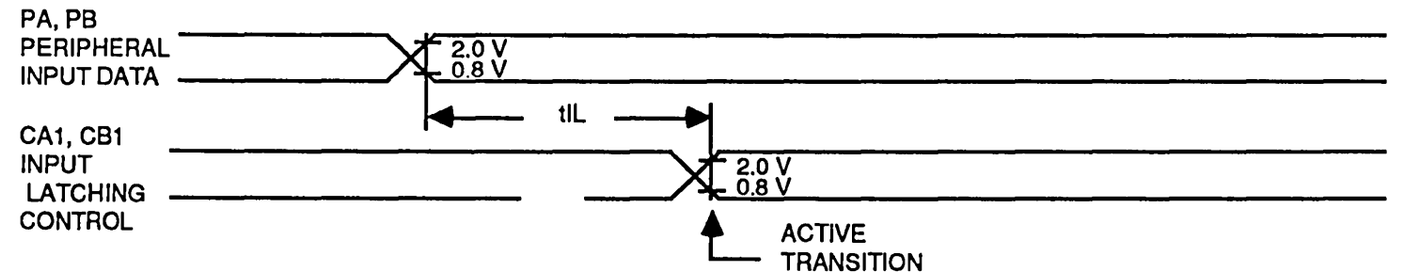


FIGURE 7. TIMING FOR SHIFT OUT WITH INTERNAL OR EXTERNAL SHIFT CLOCKING

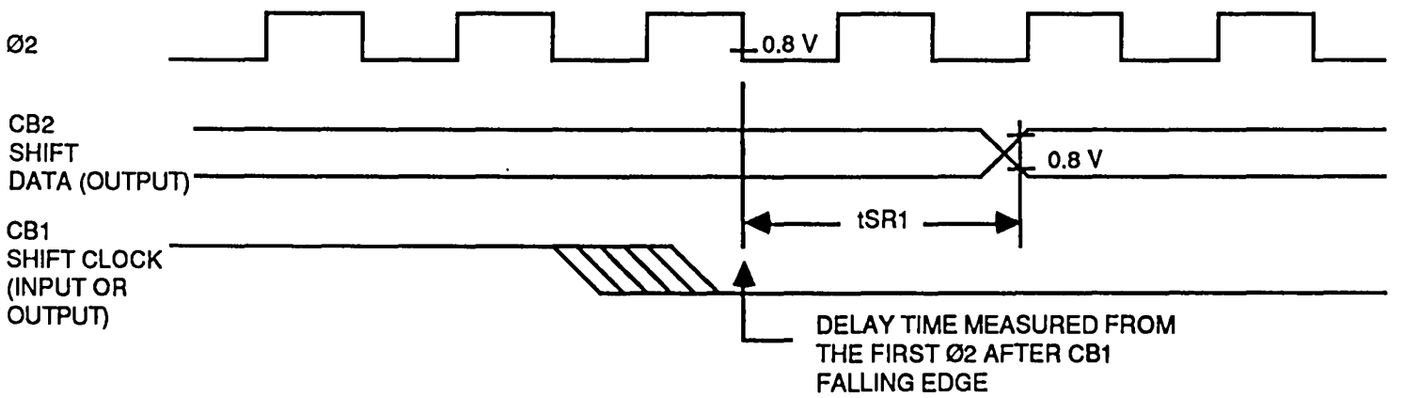


FIGURE 8. TIMING FOR SHIFT IN WITH INTERNAL OR EXTERNAL SHIFT CLOCKING (VL6522 AND VL65C22)

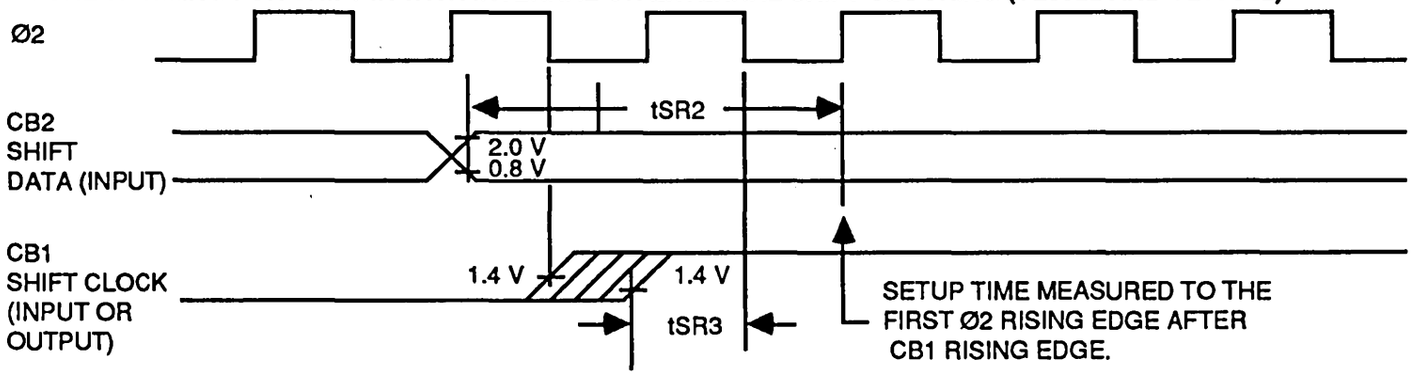


FIGURE 8A. TIMING FOR SHIFT IN WITH INTERNAL OR EXTERNAL SHIFT CLOCKING (VL65C22V)

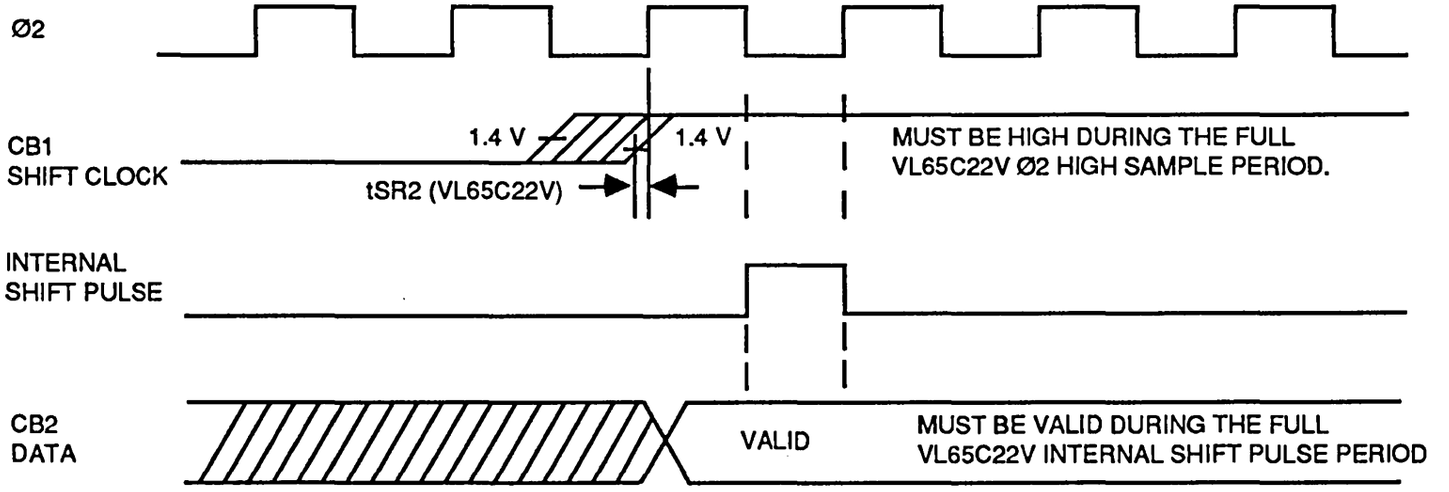


FIGURE 9. EXTERNAL SHIFT CLOCK TIMING

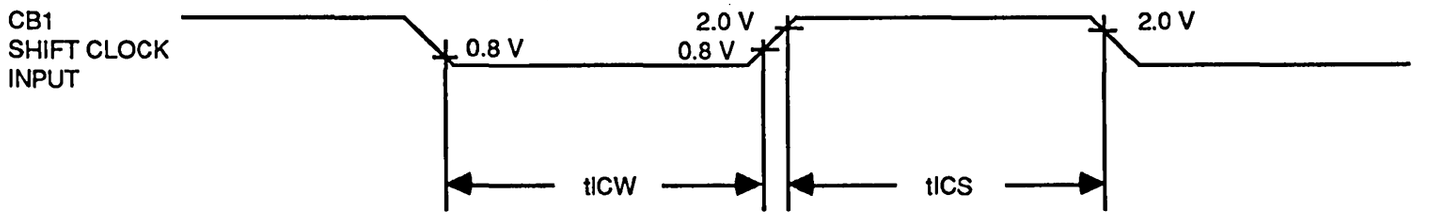


FIGURE 10. PULSE COUNT INPUT TIMING

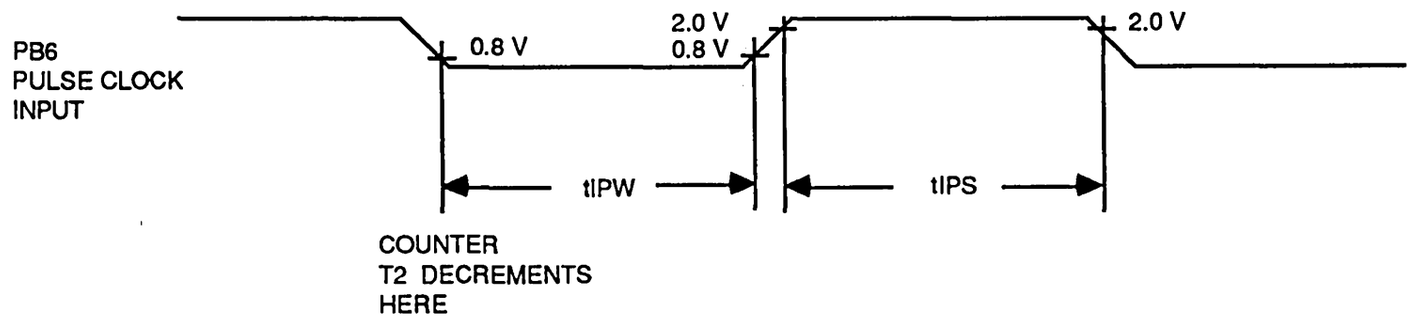


TABLE 2. REGISTER SELECT

Register Number	RS Coding				Register Designation	Register/Description	
	RS3	RS2	RS1	RS0		Write (R/–W=0)	Read (R/–W=1)
0	0	0	0	0	ORB / IRB	Output Register B	Input Register B
1	0	0	0	1	ORA / IRA	Output Register A	Input Register A
2	0	0	1	0	DDRB	Data Direction Register B	
3	0	0	1	1	DDRA	Data Direction Register A	
4	0	1	0	0	T1C - L	T1 Low-Order Latches	T1 Low-Order Counter
5	0	1	0	1	T1C - H	T1 High-Order Counter	
6	0	1	1	0	T1L - L	T1 Low-Order Latches	
7	0	1	1	1	T1L - H	T1 High-Order Latches	
8	1	0	0	0	T2C - L	T2 Low-Order Latches	T2 Low-Order Counter
9	1	0	0	1	T2C - H	T2 High-Order Counter	
10	1	0	1	0	SR	Shift Register	
11	1	0	1	1	ACR	Auxiliary Control Register	
12	1	1	0	0	PCR	Peripheral Control Register	
13	1	1	0	1	IFR	Interrupt Flag Register	
14	1	1	1	0	IER	InterruptEnable Register	
15	1	1	1	1	ORA / IRA	Output Register A *	Input Register A *

Notes: 1. * - Same as Register 1, except no handshake
2. On the VL65C22V and VL65C22, the Register Select may be decoded only while –CS2 is low.

TABLE 3. READ TIMING

Symbol	Parameter	VL6522-01		VL6522-02		VL65C22(V)-02		VL65C22(V)-04		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
tCYC	Cycle Time	1	10	0.5	10	0.5	10	0.25	10	µs
tACR	Address Setup Time	180	-	90	-	90	-	45	-	ns
tCAR	Address Hold Time	0	-	0	-	0	-	0	-	ns
tPCR	Peripheral Data Setup Time	300	-	150	-	150	-	75	-	ns
tCDR	Data Bus Delay Time	-	365	-	190	-	190	-	90	ns
tHR	Data Bus Hold Time	10	-	10	-	10	-	10	-	ns

TABLE 4. WRITE TIMING

Symbol	Parameter	VL6522-01		VL6522-02		VL65C22(V)-02		VL65C22(V)-04		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
tCYC	Cycle Time	1	10	0.5	10	0.5	10	0.25	10	µs
tC	Ø2 Pulse Width	470	-	240	-	240	-	120	-	ns
tACW	Address Setup Time	180	-	90	-	90	-	45	-	ns
tCAW	Address Hold Time	0	-	0	-	0	-	0	-	ns
tWCW	R/–W Setup Time	180	-	90	-	90	-	45	-	ns
tCWW	R/–W Hold Time	0	-	0	-	0	-	0	-	ns
tDCW	Data Bus Setup Time	200	-	90	-	90	-	45	-	ns
tHW	Data Bus Hold Time	10	-	10	-	10	-	10	-	ns
tCPW	Peripheral Data Delay Time	-	1.0	-	0.5	-	0.5	-	0.25	µs
tCMOS	Peripheral Data Delay Time to CMOS Levels	-	2.0	-	1.0	-	1.0	-	0.5	µs

Note: tRISE, tFALL = 10 to 30 ns.

FIGURE 11. READ TIMING

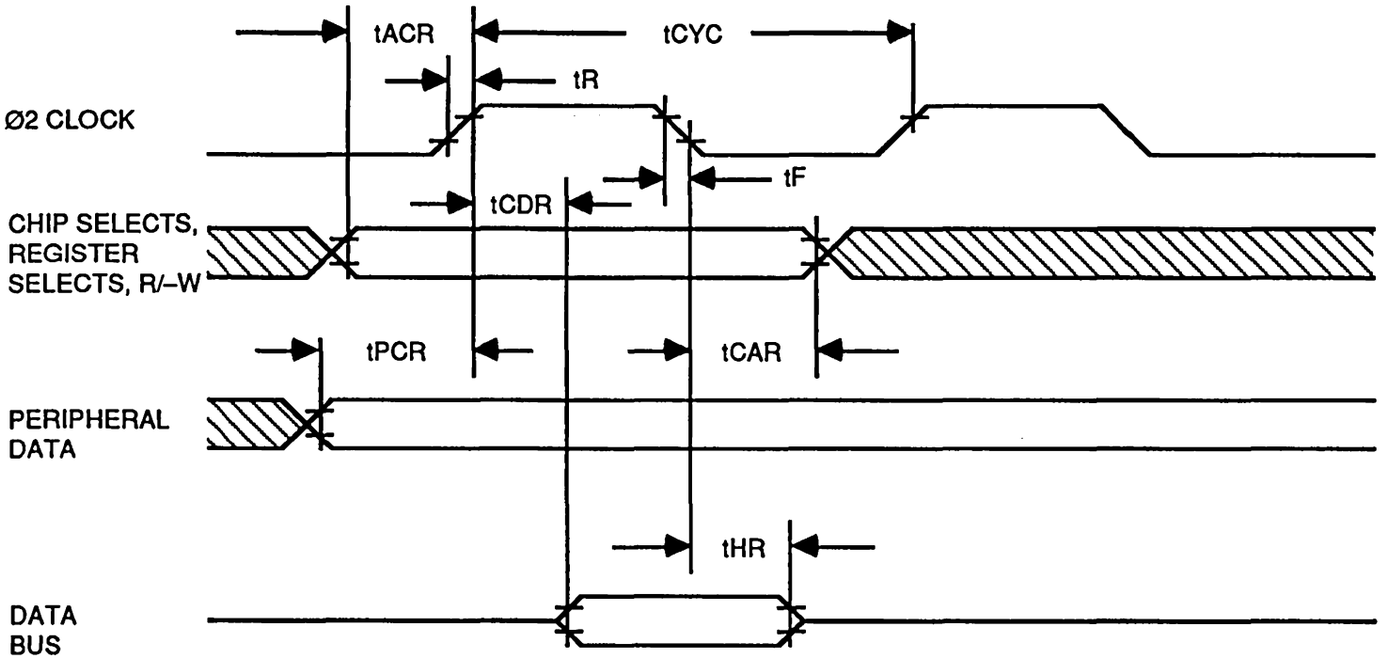


FIGURE 12. WRITE TIMING

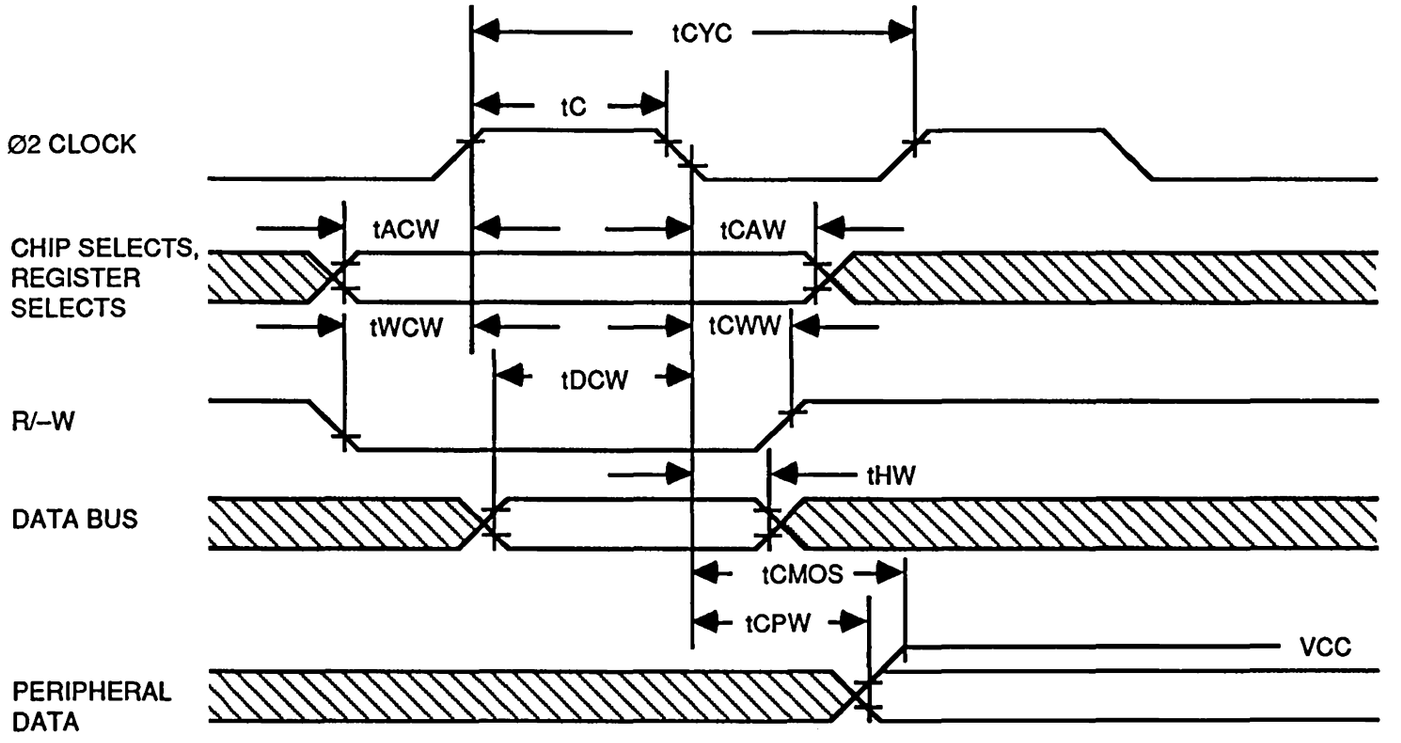
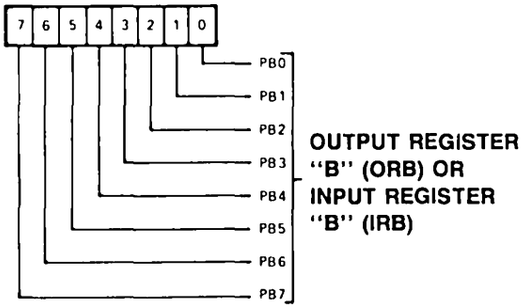
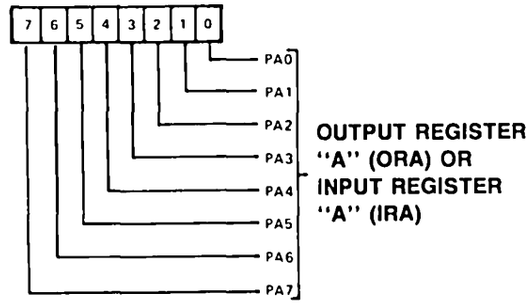


FIGURE 13. REGISTER 0, ORB/IRB



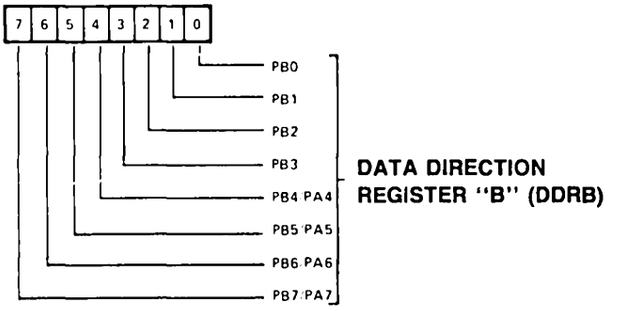
PIN DATA DIRECTION SELECTION	WRITE	READ
DDRB = "1" (OUTPUT)	MPU WRITES OUTPUT LEVEL (ORB)	MPU READS OUTPUT REGISTER BIT IN ORB. PIN LEVEL HAS NO AFFECT
DDRB = "0" (INPUT) (INPUT LATCHING DISABLED)	MPU WRITES INTO ORB, BUT NO EFFECT ON PIN LEVEL, UNTIL DDRB CHANGED	MPU READS INPUT LEVEL ON PB PIN
DDRB = "0" (INPUT) (INPUT LATCHING ENABLED)		MPU READS IRB BIT, WHICH IS THE LEVEL OF THE PB PIN AT THE TIME OF THE LAST CB1 ACTIVE TRANSITION

FIGURE 14. REGISTER 1, ORA/IRA



PIN DATA DIRECTION SELECTION	WRITE	READ
DDRA = "1" (OUTPUT) (INPUT LATCHING DISABLED)	MPU WRITES OUTPUT LEVEL (ORA)	MPU READS LEVEL ON PA PIN
DDRA = "1" (OUTPUT) (INPUT LATCHING ENABLED)		MPU READS IRA BIT WHICH IS THE LEVEL OF THE PA PIN AT THE TIME OF THE LAST CA1 ACTIVE TRANSITION
DDRA = "0" (INPUT) (INPUT LATCHING DISABLED)	MPU WRITES INTO ORA, BUT NO EFFECT ON PIN LEVEL UNTIL DDRA CHANGED	MPU READS LEVEL ON PA PIN
DDRA = "0" (INPUT) (INPUT LATCHING ENABLED)		MPU READS IRA BIT, WHICH IS THE LEVEL OF THE PA PIN AT THE TIME OF THE LAST CA1 ACTIVE TRANSITION

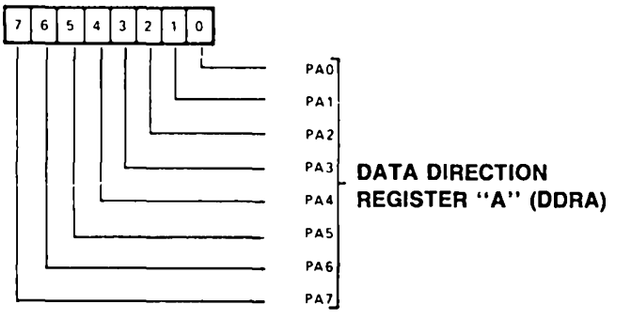
FIGURE 15. REGISTER 2, DDRB



"0" ASSOCIATED PB PIN IS AN INPUT (HIGH IMPEDANCE)

"1" ASSOCIATED PB PIN IS AN OUTPUT WHOSE LEVEL IS DETERMINED BY ORB REGISTER BIT

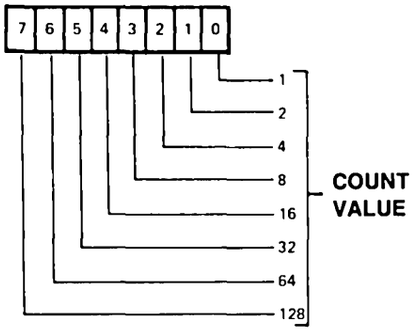
FIGURE 16. REGISTER 3, DDRA



"0" ASSOCIATED PA PIN IS AN INPUT (HIGH IMPEDANCE)

"1" ASSOCIATED PA PIN IS AN OUTPUT WHOSE LEVEL IS DETERMINED BY ORA REGISTER BIT

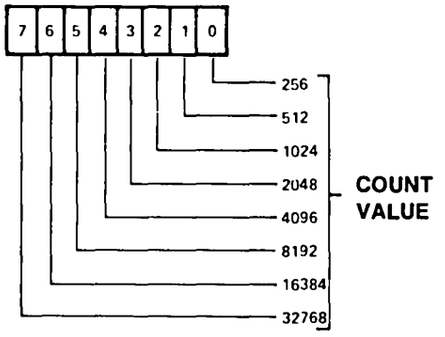
FIGURE 17. REGISTER 4, TIMER 1 LOW-ORDER COUNTER



WRITE – 8 BITS LOADED INTO T1 LOW-ORDER LATCHES. LATCH CONTENTS ARE TRANSFERRED INTO LOW-ORDER COUNTER AT THE TIME THE HIGH-ORDER COUNTER IS LOADED (REG 5).

READ – 8 BITS FROM T1 LOW-ORDER COUNTER TRANSFERRED TO MPU. IN ADDITION, T1 INTERRUPT FLAG IS RESET (BIT 6 IN INTERRUPT FLAG REGISTER).

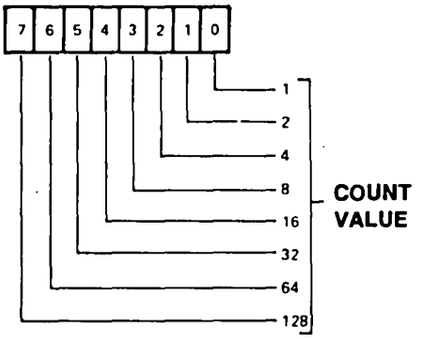
FIGURE 18. REGISTER 5, TIMER 1 HIGH-ORDER COUNTER



WRITE - 8 BITS LODED INTO T1 HIGH-ORDER LATCHES. ALSO, AT THIS TIME BOTH HIGH- AND LOW-ORDER LATCHES TRANSFERRED INTO T1 COUNTER. T1 INTERRUPT FLAG ALSO IS RESET.

READ - 8 IBTS FROM T1 HIGH-ORDER COUNTER TRANSFERRED TO MPU.

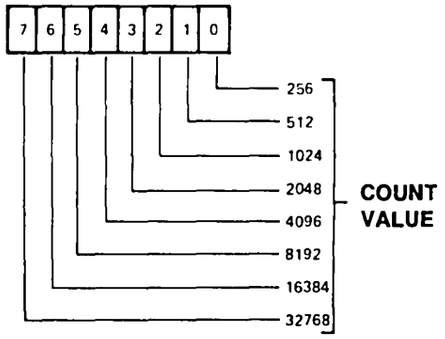
FIGURE 19. REGISTER 6, TIMER 1 LOW-ORDER LATCH



WRITE - 8 BITS LOADED INTO T1 LOW-ORDER LATCHES. THIS OPERATION IS NO DIFFERENT THAN A WRITE INTO REG 4.

READ - 8 BITS FROM T1 LOW-ORDER LATCHES TRANSFERRED TO MPU. UNLIKE REG 4 OPERATION, THIS DOES NOT CAUSE RESET OF T1 INTERRUPT FLAG

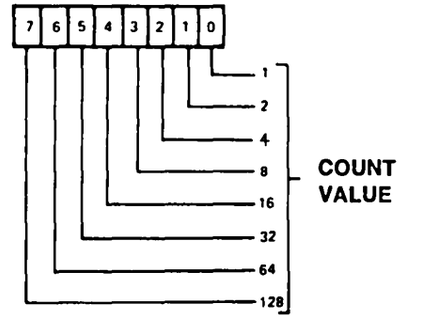
FIGURE 20. REGISTER 7, TIMER 1 HIGH-ORDER LATCH



WRITE - 8 BITS LOADED INTO T1 HIGH-ORDER LATCHES. UNLIKE REG 4 OPERATION NO LATCH-TO-COUNTER TRANSFERS TAKE PLACE.

READ - 8 BITS FROM T1 HIGH-ORDER LATCHES TRANSFERRED TO MPU.

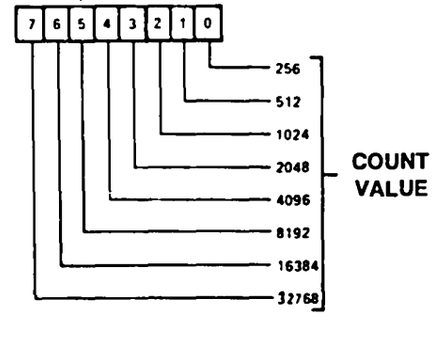
FIGURE 21. REGISTER 8, TIMER 2 LOW-ORDER LATCH/ COUNTER



WRITE - 8 BITS LOADED INTO T2 LOW-ORDER LATCH

READ - 8 BITS FROM T2 LOW-ORDER COUNTER TRANSFERRED TO MPU. T2 INTERRUPT FLAG IS RESET.

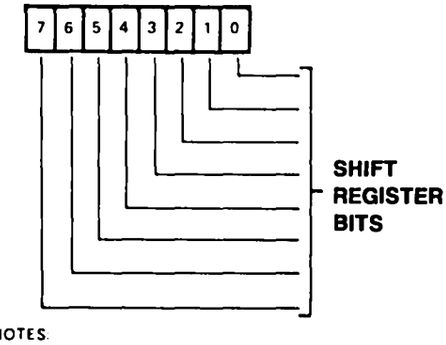
FIGURE 22. REGISTER 9, TIMER 2 HIGH-ORDER LATCH/ COUNTER



WRITE - 8 BITS LOADED INTO T2 HIGH ORDER COUNTER. ALSO, LOW ORDER LATCH TRANSFERRED TO LOW ORDER COUNTER. IN ADDITION, T2 INTERRUPT FLAG IS RESET

READ - 8 BITS FROM T2 HIGH ORDER COUNTER TRANSFERRED TO MPU

FIGURE 23. REGISTER 10, SHIFT REGISTER



NOTES:

1. WHEN SHIFTING OUT, BIT 7 IS THE FIRST BIT OUT AND SIMULTANEOUSLY IS ROTATED BACK INTO BIT 0.
2. WHEN SHIFTING IN, BITS INITIALLY ENTER BIT 0 AND ARE SHIFTED TOWARDS BIT 7.

FIGURE 24. REGISTER 11A, AUXILIARY CONTROL REGISTER

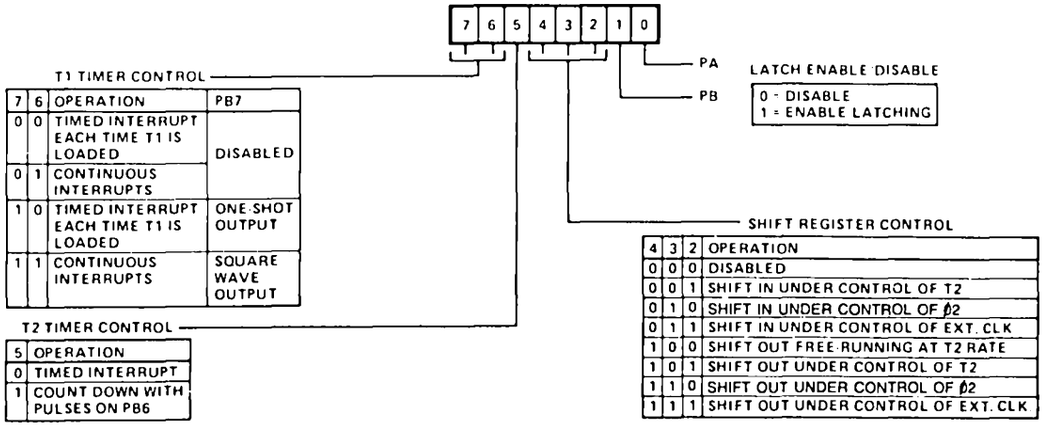
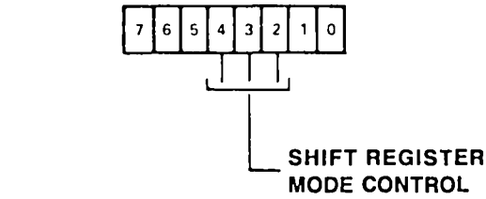


FIGURE 25. REGISTER 11B, AUXILIARY CONTROL REGISTER



4	3	2	OPERATION
0	0	0	DISABLED
0	0	1	SHIFT IN UNDER CONTROL OF T2
0	1	0	SHIFT IN UNDER CONTROL OF ϕ_2
0	1	1	SHIFT IN UNDER CONTROL OF EXT CLK
1	0	0	SHIFT OUT FREE RUNNING AT T2 RATE
1	0	1	SHIFT OUT UNDER CONTROL OF T2
1	1	0	SHIFT OUT UNDER CONTROL OF ϕ_2
1	1	1	SHIFT OUT UNDER CONTROL OF EXT CLK

FIGURE 26. REGISTER 12, PERIPHERAL CONTROL REGISTER

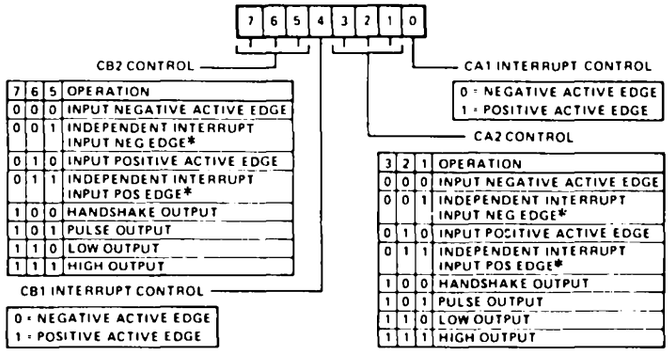
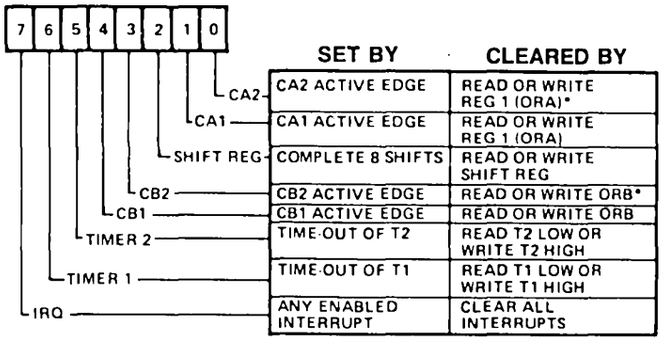


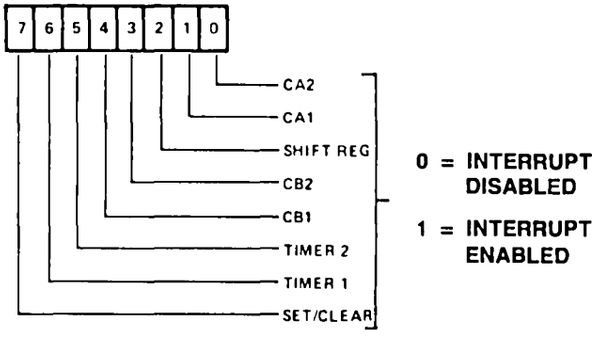
FIGURE 27. REGISTER 13, INTERRUPT FLAG REGISTER



	SET BY	CLEARED BY
CA2	CA2 ACTIVE EDGE	READ OR WRITE REG 1 (ORA)*
CA1	CA1 ACTIVE EDGE	READ OR WRITE REG 1 (ORA)
SHIFT REG	COMPLETE 8 SHIFTS	READ OR WRITE SHIFT REG
CB2	CB2 ACTIVE EDGE	READ OR WRITE ORB*
CB1	CB1 ACTIVE EDGE	READ OR WRITE ORB
TIMER 2	TIME-OUT OF T2	READ T2 LOW OR WRITE T2 HIGH
TIMER 1	TIME-OUT OF T1	READ T1 LOW OR WRITE T1 HIGH
IRQ	ANY ENABLED INTERRUPT	CLEAR ALL INTERRUPTS

* IF THE CA2/CB2 CONTROL IN THE PCR IS SELECTED AS "INDEPENDENT" INTERRUPT INPUT, THEN READING OR WRITING THE OUTPUT REGISTER ORA/ORB WILL NOT CLEAR THE FLAG BIT. INSTEAD, THE BIT MUST BE CLEARED BY WRITING INTO THE IFR, AS DESCRIBED PREVIOUSLY.

FIGURE 28. REGISTER 14, INTERRUPT ENABLE REGISTER



NOTES:
1 IF BIT 7 IS A "0", THEN EACH "1" IN BITS 0 - 6 DISABLES THE CORRESPONDING INTERRUPT.
2 IF BIT 7 IS A "1", THEN EACH "1" IN BITS 0 - 6 ENABLES THE CORRESPONDING INTERRUPT.
3 IF A READ OF THIS REGISTER IS DONE, BIT 7 WILL BE "1" AND ALL OTHER BITS WILL REFLECT THEIR ENABLE/DISABLE STATE.

ABSOLUTE MAXIMUM RATINGS

Ambient Operating Temperature	–10 to +80°C
Storage Temperature	–65 to +150°C
Supply Voltage to Ground Potential	–0.5 to +7.0 V
Applied Voltage	–0.5 to +7.0 V
Power Dissipation	750 mW

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated on the operational sections of this specification is not implied and exposure to conditions for extended periods may affect device reliability.

DC CHARACTERISTICS (VL6522): VCC = 5 V ±5%, TA = 0°C to 70°C

Symbol	Parameter		Min.	Typ	Max.	Unit	Conditions
VIH	Input High Voltage		2.4		VCC	V	
VIL	Input Low Voltage		–0.3		0.4	V	
IIN	Input Leakage Current R/–W, –RES, RS3 - RS0, –CS2, CS1, CA1,Ø2		-		±2.5	µA	VIN = 0 V to 5.0 V VCC = 0 V
ITSI	Input Leakage Current for Three-State Off D7 - D0		-		±10	µA	VIN = 0.4 V to 2.4 V VCC = 5.25 V
IIH	Input High Current PA7-PA0, CA2, PB7-PB0, CB1, CB2		–100		-	µA	VIN = 2.4 V
IIL	Input Low Current PA7-PA0, CA2, PB7-PB0, CB1, CB2		-		–1.8	mA	VIL = 0.4 V
VOH	Output High Voltage PA7-PA0, CA2, PB7-PB0, CB1, CB2		2.4		-	V	VCC = 4.75 V ILOAD = –100 µA
VOL	Output Low Voltage		-		0.4	V	VCC = 4.75 V ILOAD = 3.2 mA
IOH	Output High Current (Sourcing)	PA7-PA0, PB7-PB0 (TTL drive), D7-D0	–100		-	µA	VOH = 2.4 V
		PB7-PB0 (other drive, e.g., Darlington)	–1.0		-	mA	VOH = 1.5 V
IOL	Output Low Current (Sinking)		1.6		-	mA	VOL = 0.4 V
IOFF	Output Leakage Current (Off State) –IRQ		-		10	µA	
PD	Power Dissipation		-		700	mW	

DC CHARACTERISTICS (VL65C22 AND VL65C22V): VCC = 5 V ±5%, TA = 0°C to 70°C

Symbol	Parameter		Min.	Typ	Max.	Unit	Conditions
VIH	Input High Voltage		2.4		VCC	V	
VIL	Input Low Voltage		–0.3		0.4	V	
IIN	Input Leakage Current R/–W, –RES, RS3 - RS0, –CS2, CS1, CA1,Ø2		-		±1.0	µA	VIN = 0 V to 5.0 V VCC = 0 V
ITSI	Input Leakage Current for Three-State Off D7 - D0		-		±10	µA	VIN = 0.4 V to 2.4 V VCC = 5.25 V
IIH	Input High Current PA7-PA0, CA2, PB7-PB0, CB1, CB2		–200		-	µA	VIN = 2.4 V
IIL	Input Low Current PA7-PA0, CA2, PB7-PB0, CB1, CB2		-		–1.6	mA	VIL = 0.4 V
VOH	Output High Voltage PA7-PA0, CA2, PB7-PB0, CB1, CB2		2.4		-	V	VCC = 4.75 V ILOAD = –100 µA
VOL	Output Low Voltage		-		0.4	V	VCC = 4.75 V ILOAD = 3.2 mA
IOH	Output High Current (Sourcing)	PA7-PA0, PB7-PB0 (TTL drive), D7-D0	–200		-	µA	VOH = 2.4 V
		PB7-PB0 (other drive, e.g., Darlington)	–3.0		-	mA	VOH = 1.5 V
IOL	Output Low Current (Sinking)		1.6		-	mA	VOL = 0.4 V
IOFF	Output Leakage Current (Off State) –IRQ		-		10	µA	
ICC	Power Supply Current		-		2.5	mA/MHz	

CAPACITANCE: TA = 25°C, f = 1 MHz

Symbol	Parameter		Min.	Typ	Max.	Unit	Conditions
CI	Input Capacitance	R/–W, –RES, RS3-RS0, CS2,–CS1, D7-D0, CA1, CA2, PA7-PA0, PB7-PB0	-		7.0	pF	VCC = 5.0 V VIN = 0 V
		CB1, CB2	-		10	pF	
		Ø2 Input	-		20	pF	
COUT	Output Capacitance		-		10	pF	