μPD8255A PROGRAMMABLE PERIPHERAL INTERFACE

Description

The μPD8255A-2 and μPD8255A-5 are general purpose programmable input/output devices designed for use with the 8080A/8085A microprocessors. Twenty-four I/O lines may be programmed in two groups of twelve (group I and group II) and used in three modes of operation. In the basic mode, (Mode 0), each group of twelve I/O pins may be programmed in sets of 4 to input or output. In the strobed mode, (MODE 1), each group may be programmed to have 8 lines of input or output. Three of the remaining four pins in each group are used for handshaking strobes and interrupt control signals. The bidirectional bus mode, (MODE 2), uses the 8 lines of port A for a bi-directional bus, and five lines from port C for bus control signals.

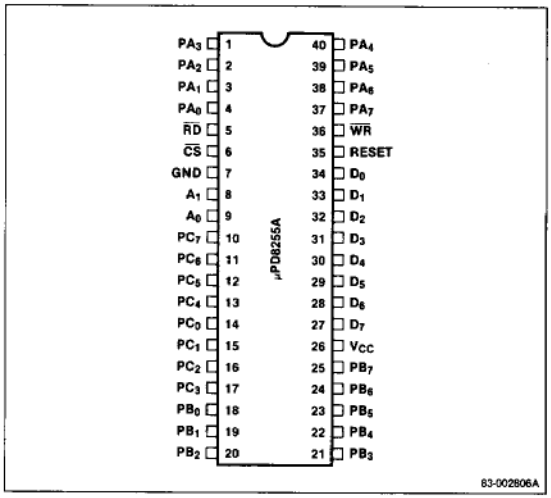
Features

- ☐ Fully compatible with the 8080A/8085 microprocessor families
- ☐ All inputs and outputs TTL compatible
- ☐ 24 programmable I/O pins
- ☐ Direct bit set/reset eases control application interfaces
- ☐ Eight Darlington drive outputs for printers and displays
- ☐ LSI drastically reduces system package count

Ordering Information

Part Number	Package Type	Max System Clock Frequency
μPD8255AC-2	40-pin plastic DIP	5 MHz
μPD8255AC-5	40-pin plastic DIP	4 MHz

Pin Configuration



Pin Identification

No.	Symbol	Function
1-4, 37-40	PA_7-PA_0	Port A (I/O)
5	$\overline{RD}$	Read input
6	$\overline{CS}$	Chip select input
7	GND	Ground
8,9	A_1,A_0	Port address inputs
10-17	PC_7-PC_0	Port C (I/O)
18-25	PB_7-PB_0	Port B (I/O)
26	V_{CC}	+5 V power supply
27-34	D_7-D_0	Bidirectional data bus
35	RESET	Reset input
36	$\overline{WR}$	Write input

8

Pin Functions

D_7-D_0 (Data Bus Buffer)

These pins form a three-state, bidirectional data bus buffer that is controlled by input and output instructions executed by the processor. Control words and status information are also transmitted via D_7-D_0.

$\overline{CS}$ (Chip Select)

A low input to this pin enables the μPD8255A for communication with the 8080A/8085A.

$\overline{RD}$ (Read)

A low input to this pin enables the μPD8255A for communication with the 8080A/8085A.

$\overline{WR}$ (Write)

A low input to this pin enables the data bus buffer to receive data or control words from the processor.

A_1, A_0 (Port Address)

These inputs are used in conjunction with $\overline{CS}$, $\overline{RD}$, and $\overline{WR}$ to control the selection of one of the three ports on the control word register. A_0 and A_1 are usually connected to A_0 and A_1 of the processor address bus.

RESET (Reset)

A high level input to this pin clears the control register and places ports A, B, and C in input mode. The input latches in ports A, B, and C are not cleared.

PA_7-PA_0, PB_7-PB_0, PC_7-PC_0 (Ports A, B, and C)

These three 8-bit I/O ports can be configured to meet a variety of functional requirements through system software. The effectiveness and flexibility of the μPD8255A are further enhanced by special features unique to each of the ports, as follows:

- Port A has an 8-bit data output latch/buffer, data input latch/buffer, and data input latch.
- Port B has an 8-bit data I/O latch/buffer and an 8-bit data input buffer.
- Port C has an 8-bit output latch/buffer and a data input buffer (input not latched).

Port C may be divided into two independent 4-bit control and status ports for use with ports A and B.

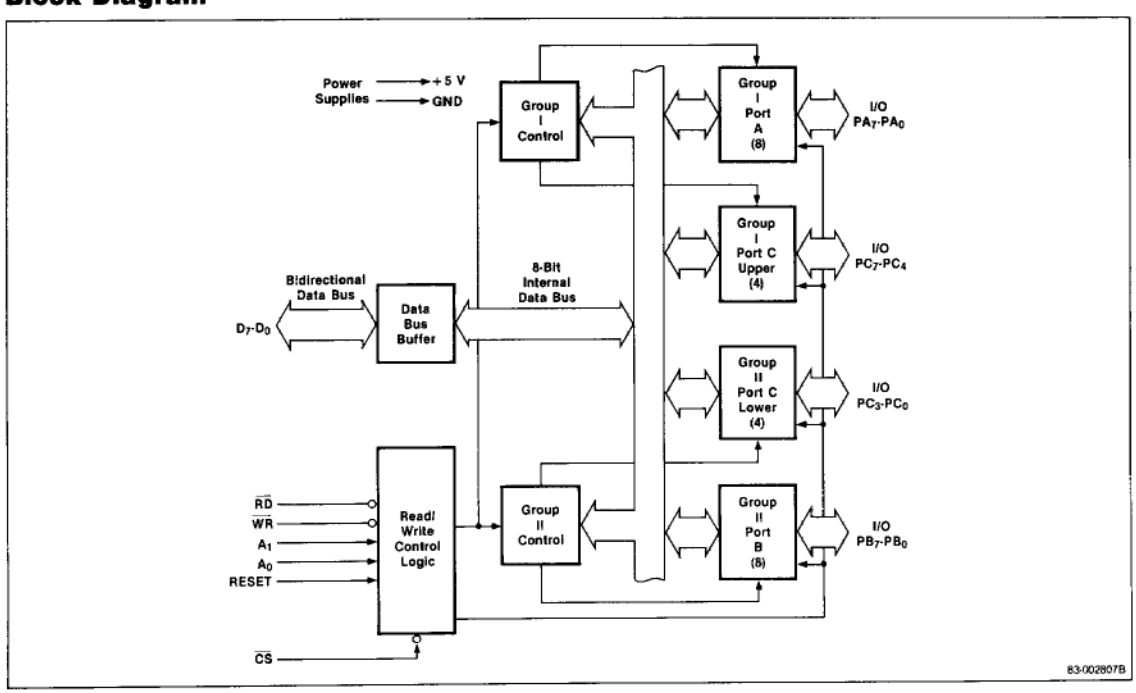
V_{CC}

+5 V power supply.

GND (Ground)

Connection to ground.

Block Diagram



Functional Description

The read/write and control logic manages all internal and external transfers of data, control, and status. It is through this block that the processor address and control buses control the peripheral interfaces.

Through an OUT instruction in system software from the processor, a control word is transmitted to the μPD8255A. Information such as the mode, bit set, and bit reset is used to initialize the functional configuration of each I/O port.

Both group I and group II accept commands from the read/write control logic and control words from the internal data bus and in turn controls its associated I/O ports, as follows:

- Group I: port A and upper port C (PC_7-PC_4)
- Group II: port B and lower port C (PC_3-PC_0)

While the control word register can be written to, the contents cannot be read back to the processor.

Absolute Maximum Ratings

T_A = 25°C

Operating temperature, T_{OPT}	0°C to +70°C
Storage temperature, T_{STG}	−65°C to +150°C
Voltage on any pin with respect to V_{SS}	−0.5 to +7 V

Comment: Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Characteristics

T_A = 0 to +70°C; V_{CC} = +5 V ±10%; V_{SS} = 0 V

		Limits			
Parameter	**Symbol**	**Min**	**Max**	**Unit**	**Test Conditions**
Input low voltage	V_{IL}	−0.5	0.8	V	
Input high voltage	V_{IH}	2	V_{CC}	V	
Output low voltage	V_{OL}		0.45	V	(2)
Output high voltage	V_{OH}	2.4		V	(3)
Darlington drive current	I_{OH} (1)	−1	−4	mA	V_{EXT} = 1.5 V R_{EXT} = 750Ω
Power supply current	I_{CC}		120	mA	V_{CC} = +5 V, output open
Input leakage current	I_{LIH}		10	μA	V_{IN} = V = V_{CC}
Input leakage current	I_{LIL}		−10	μA	V_{IN} = 0.4 V
Output leakage current	I_{LOH}		±10	μA	V_{OUT} = V_{CC}; CS = 2.0 V
Output leakage current	I_{LOL}		−10	μA	V_{OUT} = 0.4 V; CS = 2.0 V

Note:

(1) Any set of eight outputs from either port A, B, C can source 4 mA into 1.5 V.

(2) I_{OL} = 2.5 mA for DB port; 1.7 mA for peripheral ports.

(3) I_{OH} = −400μA for DB port; −200 μA for peripheral ports.

Capacitance

T_A = 25°C; V_{CC} = 0V

		Limits			
Parameter	**Symbol**	**Min**	**Max**	**Unit**	**Test Conditions**
Input capacitance	C_I		10	pF	f_c = 1 MHz
I/O capacitance	C_{IO}		20	pF	Unmeasured pins returned to V_{SS}

8

AC Characteristics

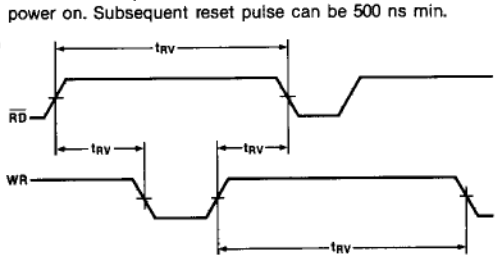
T_A = 0°C to +70°C; V_{CC} = +5 V ±5%; V_{SS} = 0 V

Parameter	Symbol	8255A-2 Limits Min	8255A-2 Limits Max	8255A-5 Limits Min	8255A-5 Limits Max	Unit	Test Conditions
Address stable before $\overline{READ}$	t_{AR}	0		0		ns	
Address stable after $\overline{READ}$	t_{RA}	0		0		ns	
$\overline{READ}$ pulse width	t_{RR}	200		250		ns	
Data valid from $\overline{READ}$	t_{RD}		140		170	ns	C_L = 150 pF
Data float after $\overline{READ}$	t_{DF}		100		100	ns	C_L = 100 pF
		10		10		ns	C_L = 15 pF
Time between $\overline{READ}$s and /$\overline{WRITE}$s	t_{RV}	200		850		ns	(Note 2)
Write							
Address stable before $\overline{WRITE}$	t_{AW}	0		0		ns	
Address stable after $\overline{WRITE}$	t_{WA}	20		20		ns	
$\overline{WRITE}$ pulse width	t_{WW}	200		250		ns	
Data valid to $\overline{WRITE}$ (T.E.)	t_{DW}	100		100		ns	
Data valid after $\overline{WRITE}$	t_{WD}	0		0		ns	
Other Timing							
$\overline{WR}$ = 0 to output	t_{WB}		350		350	ns	C_L = 150 pF
Peripheral data before $\overline{RD}$	t_{IR}	0		0		ns	
Peripheral data after $\overline{RD}$	t_{HR}	0		0		ns	
$\overline{ACK}$ pulse width	t_{AK}	300		300		ns	
$\overline{STB}$ pulse width	t_{ST}	350		350		ns	
Per. data before T.E. of $\overline{STB}$	t_{PS}	0		0		ns	
Per. data after T.E. of $\overline{STB}$	t_{PH}	150		150		ns	
$\overline{ACK}$ = 0 to output	t_{AD}		300		300	ns	C_L = 150 pF
$\overline{ACK}$ = 0 to output float	t_{KD}		250		250	ns	C_L = 50 pF
		20		20			C_L = 15 pF
$\overline{WR}$ = 1 to OBF = 0	t_{WOB}		300		650	ns	
$\overline{ACK}$ = 0 to OBF = 1	t_{AOB}		350		350	ns	
$\overline{STB}$ = 0 to IBF = 1	t_{SIB}		300		300	ns	
$\overline{RD}$ = 1 to IBF = 0	t_{RIB}		300		300	ns	
$\overline{RD}$ = 0 to INTR = 0	t_{RIT}		400		400	ns	
$\overline{STB}$ = 1 to INTR = 1	t_{SIT}		300		300	ns	C_L = 150 pF
$\overline{ACK}$ = 1 to INTR = 1	t_{AIT}		350		350	ns	
$\overline{WR}$ = 0 to INTR = 0	t_{WIT}		450		850	ns	C_L = 150 pF (Note 3)

Note:

(1) Period of reset pulse must be at least 50 μs during or after power on. Subsequent reset pulse can be 500 ns min.

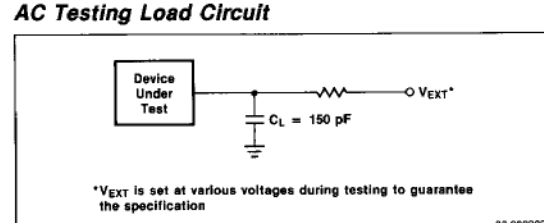
(2)



83-002808A

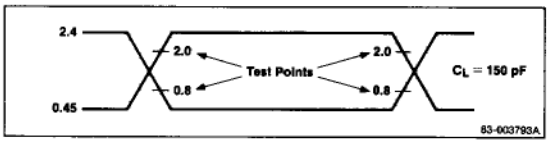
(3) INTR↑ may occur as early as $\overline{WR}$↓.

AC Testing Load Circuit

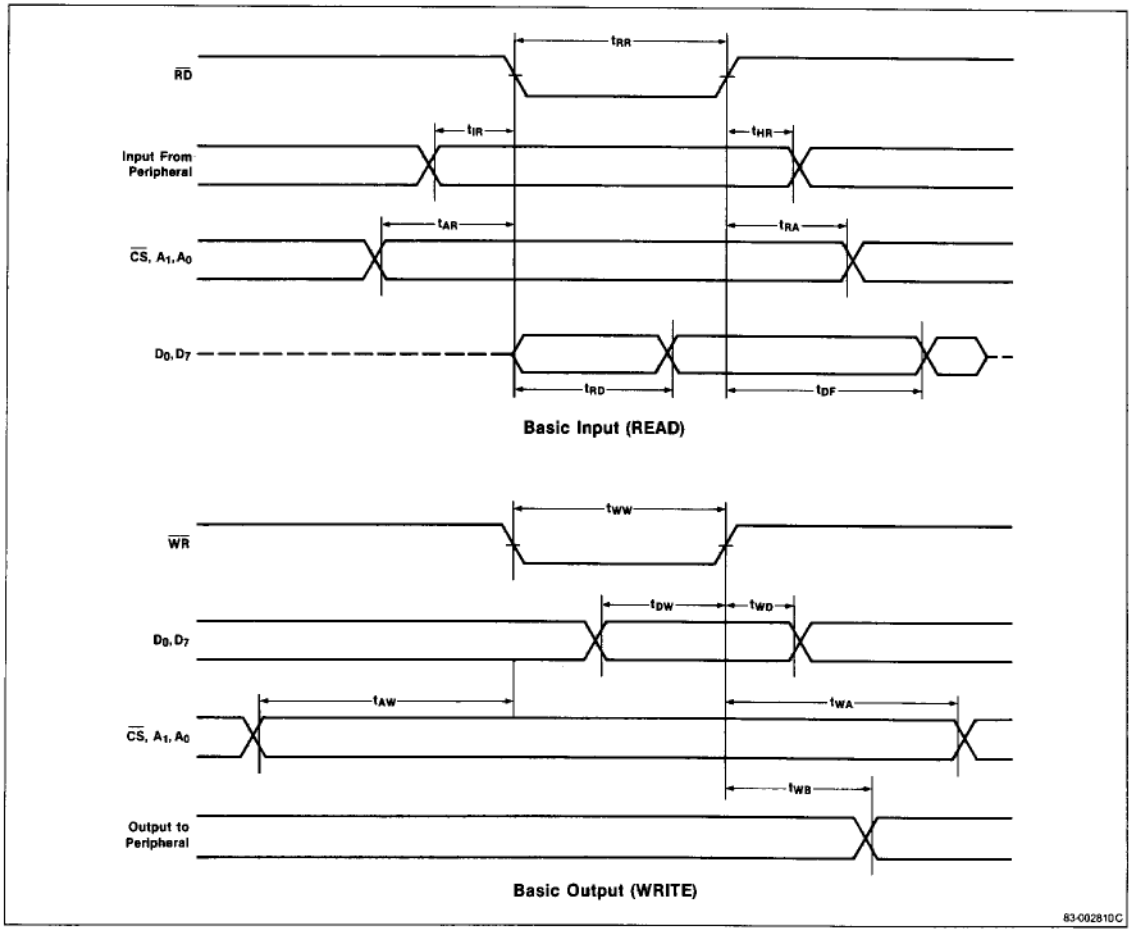


Timing Waveforms

AC Testing Input, Output Waveform



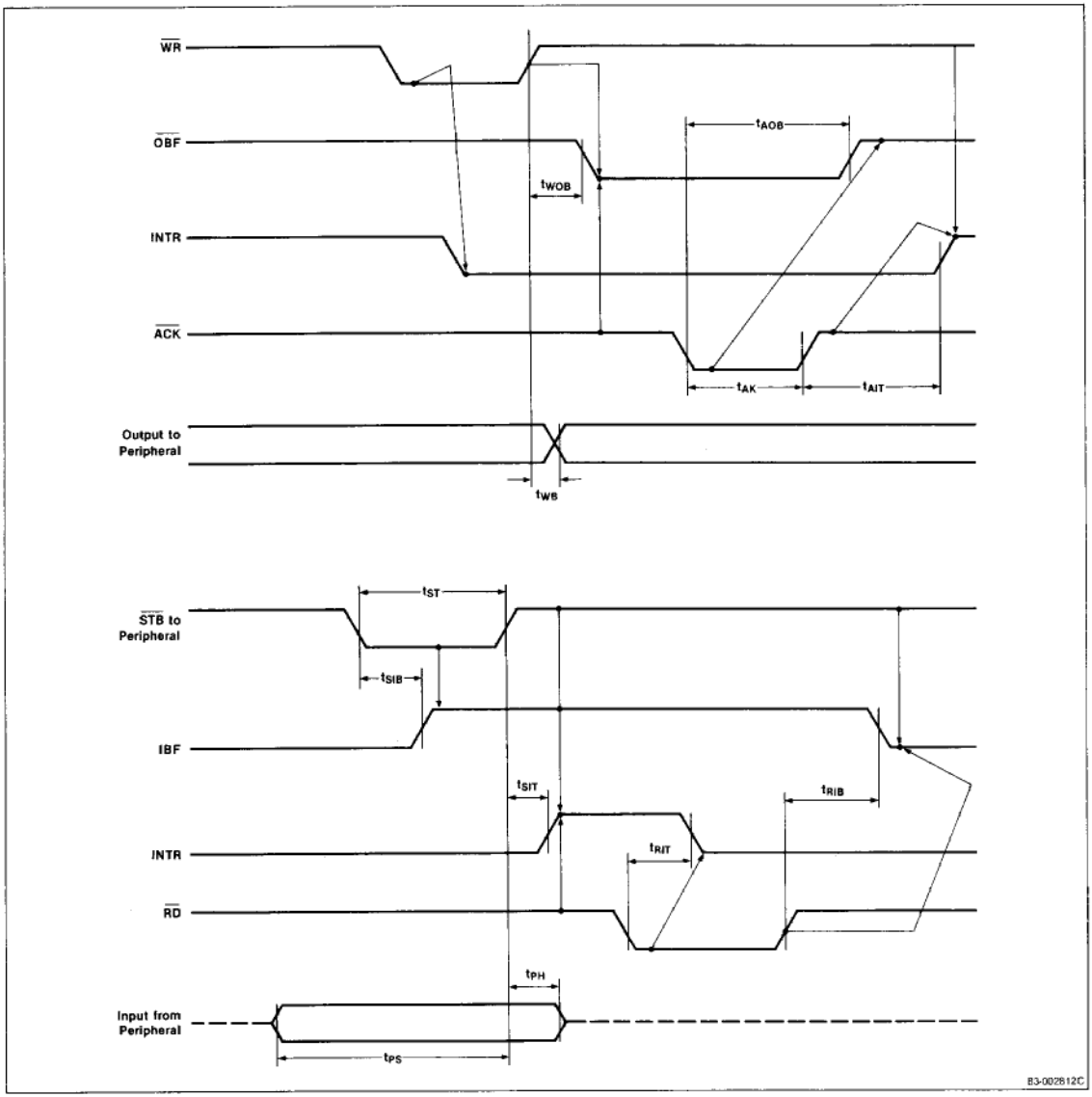
Mode 0



8

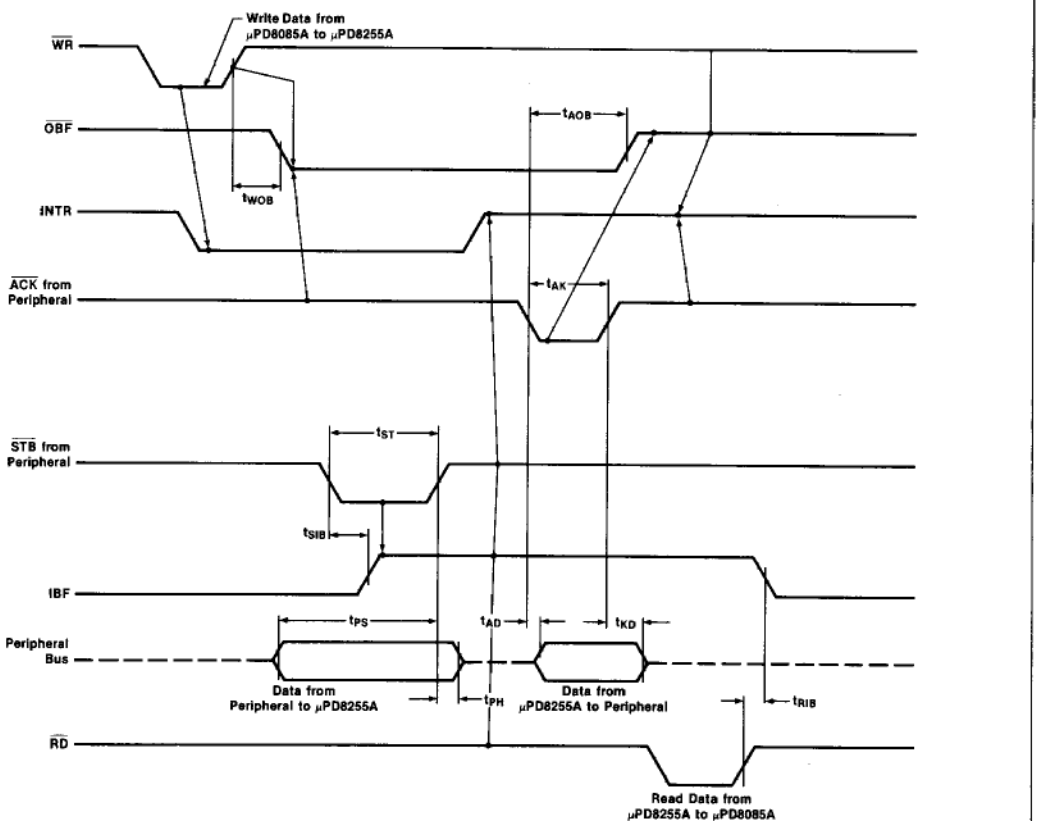
Timing Waveforms (cont)

Mode 1



Timing Waveforms (cont)

Mode 2



Note:

(1) Any sequence where $\overline{WR}$ occurs before $\overline{ACK}$ and $\overline{STB}$ occurs before $\overline{RD}$ is permissible (INTR = IBF • MASK • STB • RD + OBF • MASK • ACK • WR).

(2) When the μPD8255A is set to Mode 1 or 2, $\overline{OBF}$ is reset to be high (logic 1).

83-002813C

8

Modes

The μPD8255A can be operated in modes 0, 1 or 2 which are selected by appropriate control words and are detailed below.

Mode 0

Mode 0 provides basic input and output operations through each of the ports A, B, and C. Output data is latched and input data follows the peripheral. No "handshaking" strobes are needed.

- 16 different configurations in mode 0
- Two 8-bit ports and two 4-bit ports
- Inputs are not latched
- Outputs are latched

Mode 1

Mode 1 provides for strobed input and output operations with data transferred through port A or B and handshaking through port C.

- Two I/O groups (I and II)
- Both groups contain an 8-bit data port and a 4-bit control/data port
- Both 8-bit data ports can be either latched input or latched output

Mode 2

Mode 2 provides for strobed bidirectional operation using $PA_0PA_{.7}$ as the bidirectional latched data bus. PC_3PC_7 is used for interrupts and "handshaking" bus flow control similar to mode 1. Note that PB_0PB_7 and PC_0PC_2 may be defined as mode 0 or 1, input or output in conjunction with port A in mode 2.

- An 8-bit latched bidirectional bus port (PA_0-PA_7) and a 5-bit control port (PC_3PC_7)
- Both inputs and outputs are latched
- An additional 8-bit input or output port with a 3-bit control port.

Basic Operation

Input Operation (Read)

A_1	A_0	RD	WR	CS	
0	0	0	1	0	PORT A → DATA BUS
0	1	0	1	0	PORT B → DATA BUS
1	0	0	1	0	PORT C → DATA BUS

Output Operation (Write)

A_1	A_0	RD	WR	CS	
0	0	1	0	0	DATA BUS → PORT A
0	1	1	0	0	DATA BUS → PORT B
1	0	1	0	0	DATA BUS → PORT C
1	1	1	0	0	DATA BUS → CONTROL

Disable Function

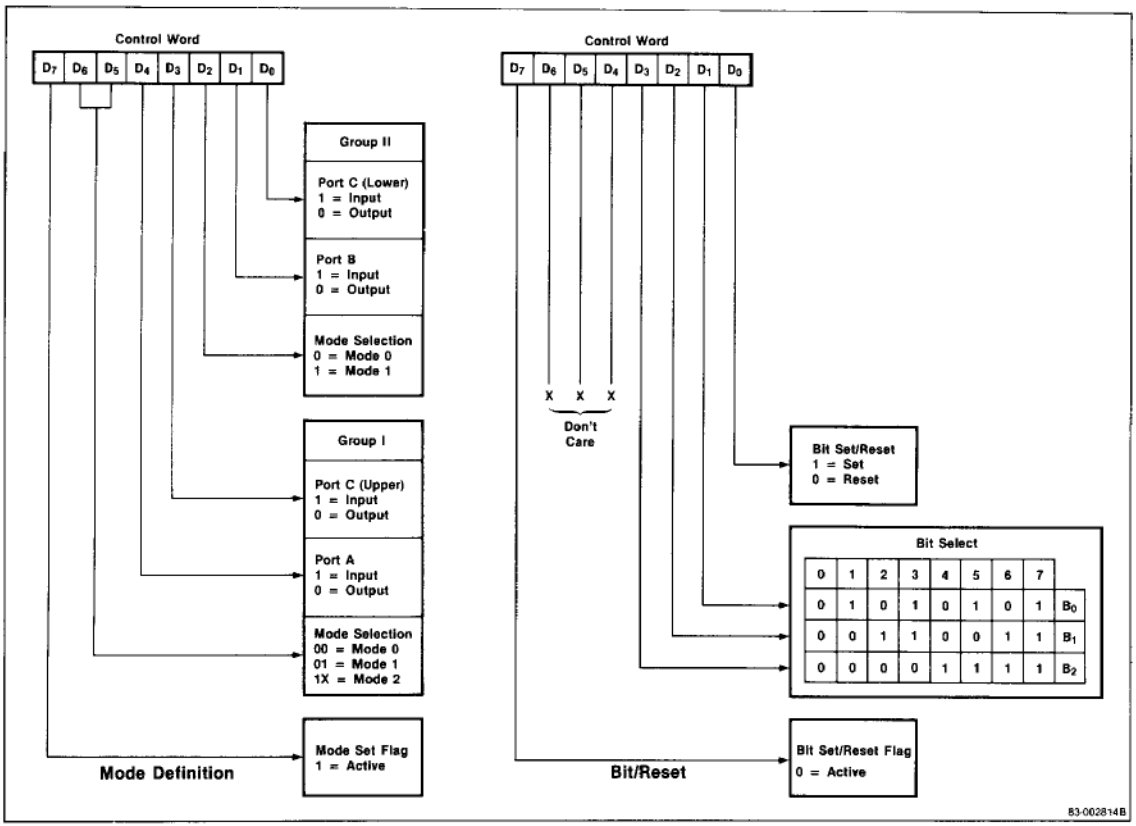
A_1	A_0	RD	WR	CS	
X	X	X	X	1	DATA BUS → HIGH Z STATE
X	X	1	1	0	DATA BUS → HIGH Z STATE

Note:

(1) X means "DO NOT CARE"
(2) All conditions not listed are illegal and should be avoided.

Formats

Mode Definition, Bit/Rest Format



8