GLC555/556

CMOS GENERAL PURPOSE TIMER

Description

The GLC555/6 are CMOS RC timers providing significantly improved performance over the standard SE/NE555/6 and 355 timers, while at the same time being direct replacements for those devices in most applications Improved parameters include low supply current, wide operating supply voltage range, low THRESHOLD, $\overline{\text{TRIGGER}}$ and $\overline{\text{RESET}}$ currents, no crowbarring of the supply current during output transitions, higher frequency performance and no requirement to decouple CONTROL VOLTAGE for stable operation

Specifically, the GLC555/6 are stable controllers capable of producing accurate time delays or frequencies The GLC556 is a dual GLC555, with the two timers operating independently of each other, sharing only V⁺ and GND In he one shot mode, the pulse width of each circuit is precisely controlled by one external resistor and capacitor. For astable operation as an oscillator, the free running frequency and the duty cycle are both accurately controlled by two external resistors and capacitor

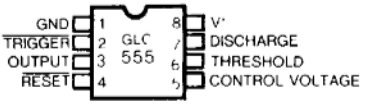
Features

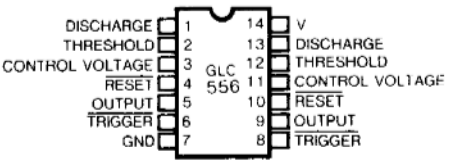
- **Exact equivalent in most cases for SE/NE555/556**
- **Low Supply Current – 80μA/160μA Typ (GLC555/556)**
- **Extremely low trigger, threshold and reset currents – 20pA Typ.**
- **High speed operation – 500 kHz guaranteed**
- **Wide operation supply voltage range – 2 to 18 volts**
- **Can be used with higher impedance timing elements than regular 555/6 for longer RC time constants.**
- **Timing from microseconds through hours**
- **Operates in both astable and monostable modes**
- **Adjustable duty cycle**
- **High output source/sink driver can drive TTL/CMOS**
- **Typical temperature stability of 0.005% per °C at 25°C**
- **Output have very low offsets, HI and LO**

Application

- Precision Timing
- Pulse Generation
- Sequential Timing
- Time Delay Generation
- Pulse Width Modulation
- Pulse Position Modulation
- Missing Pulse Detector

Pin Configuration



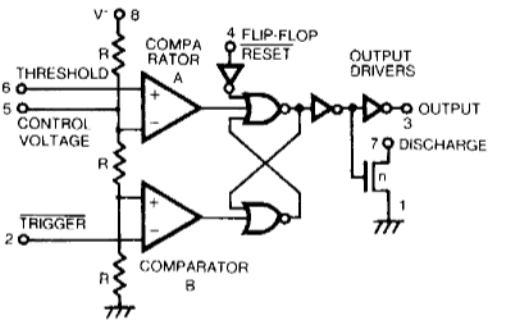


Truth Table

THRESHOLD VOLTAGE	TRIGGER VOLTAGE	$\overline{\text{RESET}}$	OUTPUT	DISCHARGE SWITCH
DON'T CARE	DON'T CARE	LOW	LOW	ON
>2/3(V⁺)	>1/3(V⁺)	HIGH	LOW	ON
V_{TH}<2/3	1/3<V_{TR}	HIGH	STABLE	STABLE
DON'T CARE	<1/3(V⁺)	HIGH	HIGH	OFF

NOTE $\overline{\text{RESET}}$ will dominate all other inputs
$\overline{\text{TRIGGER}}$ will dominate over THRESHOLD

Block Diagram



This block diagram reduces the circuitry down to its simplest equivalent components Tie down unused inputs
R=100kΩ ±20% typ

Absolute Maximum Ratings (Note 1)

Supply Voltage	V_{CC}	+18 Volts
Input Voltage (Trigger, Threshold, Reset)		$\leq V^+ + 0.3V$ to $\geq V^- - 0.3V$
Output Current	I_O	100mA
Power Dissipation(GLC555/556[2])	P_D	200/300 mW
Operating Temperature[3]	T_{OPR}	−20° to +85°C
Storage Temperature	T_{STG}	−65° to +150°C
Lead Temperature (60 Seconds)	T_{SOLDER}	300°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended period may affect device reliability.

Operating Characteristics (T_A=25°C, V^+=+2 to +15 Volts unless other specified)

SYMBOL	PARAMETER	TEST CONDITIONS		VALUE MIN	VALUE TYP	VALUE MAX	UNITS
V^+	Supply Voltage	−20°C≤T_A≤+70°C		2		18	V
I^+	Supply Current (NOTE 3)	GLC555	V^+= 2V		60	200	µA
			V^+=18V		120	300	µA
		GLC556	V^+= 2V		120	400	µA
			V^+=18V		240	600	µA
	Timing Error	R_A, R_B=1k to 100K, 5V≤V^+≤15V, C=0.1µF					
	Initial Accuracy	Note 4			2.0	5.0	%
	Drift with Temperature	Note 4	V^+= 5V		50	200	ppm/°C
			V^+=10V			300	
			V^+=15V			600	
	Drift with Supply Voltage	V^+=5V			1.0	3.0	%/V
V_{TH}	Threshold Voltage		V^+=5V	0.65	0.67	0.69	V^+
V_{TRIG}	Trigger Voltage		V^+=5V	0.31	0.33	0.35	V^+
I_{TRIG}	Trigger Current	V^+=18V			50		pA
		V^+= 5V			10		pA
		V^+= 2V			1		pA
I_{TH}	Threshold Current	V^+=18V			50		pA
		V^+= 5V			10		pA
		V^+= 2V			1		pA
I_{RST}	Reset Current	V_{RESET}=Ground	V^+=18V		100		pA
			V^+= 5V		20		pA
			V^+= 2V		2		pA
V_{RST}	Reset Voltage	V^+=18V		0.4	0.7	1.0	V
		V^+= 2V		0.4	0.7	1.0	V
V_{CV}	Control Voltage Lead			0.65	0.67	0.69	V^+
V_O	Output Voltage Drop	Output Lo	V^+=15V I_{SINK}=20mA		0.4	1.0	V
			V^+= 5V I_{SINK}=3.2mA		0.2	0.4	V
		Output Hi	V^+=15V I_{SOURCE}=0.8mA	14.3	14.6		V
			V^+= 5V I_{SOURCE}=0.8mA	4.0	4.3		
t_r	Rise Time of Output	R_L=10MΩ	C_L=10pF V^+=5V	35	40	75	ns
t_f	Fall Time of Output	R_L=10MΩ	C_L=10pF V^+=5V	35	40	75	ns
f_{max}	Guaranteed Max Osc Freq	Astable Operation		500			kHz

NOTE

1. Due to the SCR structure inherent in the CMOS process used to fabricate these devices, connecting any terminal to a voltage greater than V^+ +0.3V or less than V− 0.3V may cause destructive latchup. For this reason it is recommended that no inputs from external sources, not operating from the same power supply, be applied to the device before its power supply is established. In multiple systems, the supply of the GLC555/6 must be turned on first.
2. Junction temperatures should not exceed 135°C and the power dissipation must be limited to 20mW at 125°C. Below 125°C power dissipation may be increased to 300mW at 25°C. Derating factor is approximately 3mW/°C (GLC556) or 2mW/°C (GLC555).
3. The supply current value is essentially independent of the TRIGGER, THRESHOLD and RESET voltages.
4. Parameter is not 100% tested. Majority of all units meet this specification.

Application Notes

GENERAL

The GLC555/6 devices are, in most instances, direct replacements for the NE/SE 555/6 devices However, it is possible to effect economies in the external component count using the GLC555/6 Because the bipolar 555/6 devices produce large crowbar currents in the output driver, it is necessary to decouple the power supply lines with a good capacitor close to the device. The GLC555/6 devices produce no such transients See Figure 2

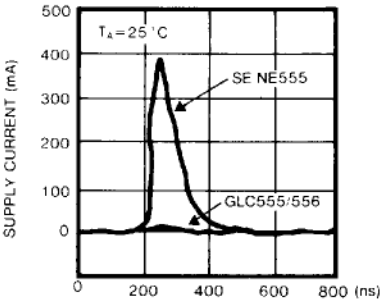


Figure 2. Supply Current Transient Compared with a Standard Bipolar 555 During an Output Transition

The GLC555/556 produces supply current spikes of only 2-3 mA instead of 300-400mA and supply decoupling is normally not necessary Secondly, in most instances, the CONTROL VOLTAGE decoupling capacitors are not required since the input impedance of the CMOS comparators on chip are very high Thus, for many applications 2 capacitors can be saved using a GLC555 and 3 capacitors with a GLC555 .

POWER SUPPLY CONSIDERATIONS

Although the supply current consumed by the GLC555/6 devices is very low, the total system supply can be high unless the timing components are high impedance Therefore, use high values for R and low values for C in Figures 3 and 4

OUTPUT DRIVE CAPABILITY

The output driver consists of a CMOS inverter capable of driving most logic families including CMOS and TTL As such, if driving CMOS, the output swing at all supply voltages will equal the supply voltage At a supply voltage of 4 5 volts or more the GLC555/6 will drive at least 2 standard TTL loads

ASTABLE OPERATION

The circuit can be connected to trigger itself and free run as a multivibrator see Figure 3 The output swings from rail to rail, and is a true 50% duty cycle square wave (Trip points and output swings are symmetrical) Less than a 1% frequency variation is observed, over a voltage range of +5 to +15V

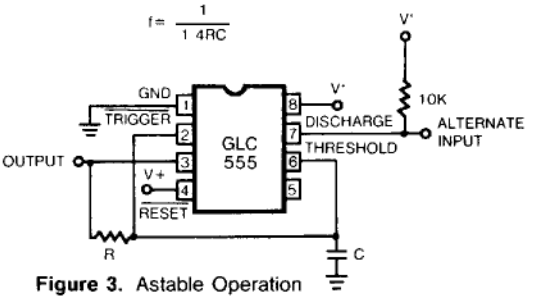


Figure 3. Astable Operation

MONOSTABLE OPERATION

In this mode of operation, the timer functions as a one-shot. Initially the external capacitor (C) is held discharged by a transistor inside the timer Upon application of a negative $\overline{\text{TRIGGER}}$ pulse to pin 2 the internal flip flop is set which releases the short circuit across the external capacitor and drives the OUTPUT high The voltage across the capacitor now increases exponentially with a time constant $t=R_AC$ When the voltage across the capacitor equals 2/3 V+, the comparator resets the flip flop, which in turn discharges the capacitor rapidly and also drives the OUTPUT to its low state $\overline{\text{TRIGGER}}$ must return to a high state before the OUTPUT can return to a low state

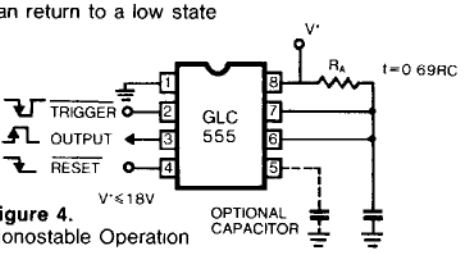


Figure 4. Monostable Operation

CONTROL VOLTAGE

The CONTROL VOLTAGE terminal permits the two trip voltages for the THRESHOLD and $\overline{\text{TRIGGER}}$ internal comparators to be controlled This provides the possibility of oscillation frequency modulation in the astable mode or even inhibition of oscillation, depending on the applied voltage In the monostable mode, delay times can be changed by varying the applied voltage to the CONTROL VOLTAGE pin.

$\overline{\text{RESET}}$

The $\overline{\text{RESET}}$ terminal is designed to have essentially the same trip voltage as the standard bipolar 555/6, i e 0 6 to 0 7 volts At all supply voltages it represents an extremely high input impedance The mode of operation of the $\overline{\text{RESET}}$ function is, however, much improved over the standard bipolar 555/6 in that it controls only the internal flip flop, which in turn controls simultaneously the state of the OUTPUT and DISCHARGE pins This avoids the multiple threshold problems sometimes encountered with slow falling edges in the bipolar devices