MC54/74HC646

Octal 3-State Bus Transceivers and D Flip-Flops

High–Performance Silicon–Gate CMOS

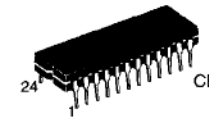
The MC54/74HC646 is identical in pinout to the LS646. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

These devices are bus transceivers with D flip–flops. Depending on the status of the Data–Source Selection pins, data may be routed to the outputs either from the flip–flops or transmitted real–time from the inputs (see Function Table and Application Information).

The Output Enable and the Direction pins control the transceiver's function. Bus A and Bus B cannot be routed as outputs to each other simultaneously, but can be routed as inputs to the A and B flip–flops. Also, the A and B flip–flops can be routed as outputs to Bus A and Bus B. Additionally, when either or both of the ports are in the high–impedance state, these I/O pins may be used as inputs to the D flip–flops for data storage.

The user should note that because the clocks are not gated with the Direction and Output Enable pins, data at the A and B ports may be clocked into the storage flip–flops at any time.

- Output Drive Capability: 15 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1 µA
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 780 FETs or 195 Equivalent Gates



J SUFFIX
CERAMIC PACKAGE
CASE 758–02

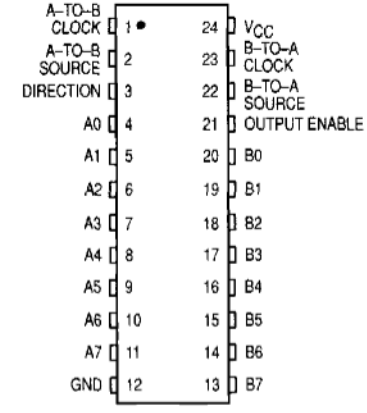
N SUFFIX
PLASTIC PACKAGE
CASE 724–03

DW SUFFIX
SOIC PACKAGE
CASE 751E–04

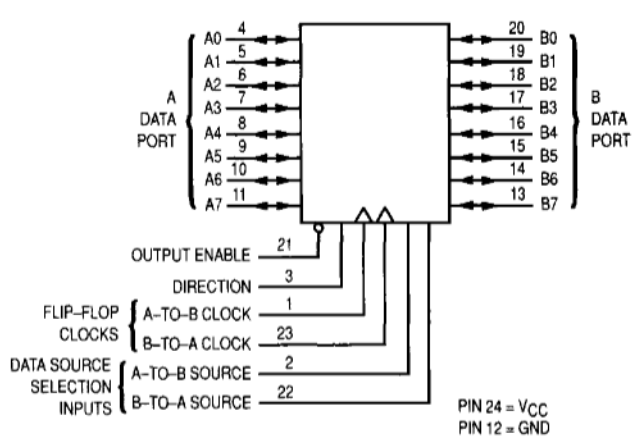
ORDERING INFORMATION

MC54HCXXXJ	Ceramic
MC74HCXXXN	Plastic
MC74HCXXXDW	SOIC

PIN ASSIGNMENT



LOGIC DIAGRAM



MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	– 0.5 to + 7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	– 1.5 to V_{CC} + 1.5	V
$V_{I/O}$	DC I/O Voltage (Referenced to GND)	– 0.5 to V_{CC} + 0.5	V
I_{in}	DC Input Current, per Pin	± 20	mA
$I_{I/O}$	DC I/O Current, per Pin	± 35	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	± 75	mA
P_D	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package†	750 500	mW
T_{stg}	Storage Temperature	– 65 to + 150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	 260 300	°C

* Maximum Ratings are those values beyond which damage to the device may occur.
Functional operation should be restricted to the Recommended Operating Conditions.

†Derating — Plastic DIP: – 10 mW/°C from 65° to 125°C
Ceramic DIP: – 10 mW/°C from 100° to 125°C
SOIC Package: – 7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 2.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range GND ≤ (V_{in} or V_{out}) ≤ V_{CC}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open. I/O pins must be connected to a properly terminated line or bus.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)		2.0	6.0	V
V_{in}, V_{out}	DC Input Voltage, Output Voltage (Referenced to GND)		0	V_{CC}	V
T_A	Operating Temperature, All Package Types		– 55	+ 125	°C
t_r, t_f	Input Rise and Fall Time (Figure 1)	V_{CC} = 2.0 V	0	1000	ns
		V_{CC} = 4.5 V	0	500	
		V_{CC} = 6.0 V	0	400	

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit			Unit
				– 55 to 25°C	≤ 85°C	≤ 125°C	
V_{IH}	Minimum High–Level Input Voltage	V_{out} = 0.1 V or V_{CC} – 0.1 V $\|I_{out}\|$ ≤ 20 μA	2.0 4.5 6.0	1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	V
V_{IL}	Maximum Low–Level Input Voltage	V_{out} = 0.1 V or V_{CC} – 0.1 V $\|I_{out}\|$ ≤ 20 μA	2.0 4.5 6.0	0.3 0.9 1.2	0.3 0.9 1.2	0.3 0.9 1.2	V
V_{OH}	Minimum High–Level Output Voltage	V_{in} = V_{IH} or V_{IL} $\|I_{out}\|$ ≤ 20 μA	2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
		V_{in} = V_{IH} or V_{IL} $\|I_{out}\|$ ≤ 6.0 mA $\|I_{out}\|$ ≤ 7.8 mA	4.5 6.0	3.98 5.48	3.84 5.34	3.70 5.20	
V_{OL}	Maximum Low–Level Output Voltage	V_{in} = V_{IH} or V_{IL} $\|I_{out}\|$ ≤ 20 μA	2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		V_{in} = V_{IH} or V_{IL} $\|I_{out}\|$ ≤ 6.0 mA $\|I_{out}\|$ ≤ 7.8 mA	4.5 6.0	0.26 0.26	0.33 0.33	0.40 0.40	
I_{in}	Maximum Input Leakage Current	V_{in} = V_{CC} or GND (Pins 1, 2, 3, 21, 22, and 23)	6.0	± 0.1	± 1.0	± 1.0	μA

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DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC} V	– 55 to 25°C	≤ 85°C	≤ 125°C	Unit
I_{OZ}	Maximum Three–State Leakage Current	Output in High–Impedance State $V_{in} = V_{IL}$ or V_{IH} $V_{out} = V_{CC}$ or GND, I/O Pins	6.0	±0.5	±5.0	±10	μA
I_{CC}	Maximum Quiescent Supply Current (per Package)	$V_{in} = V_{CC}$ or GND $I_{out} = 0$ μA	6.0	8	80	160	μA

NOTE: Information on typical parametric values can be found in Chapter 2.

AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 6 ns)

Symbol	Parameter	V_{CC} V	Guaranteed Limit			Unit
			– 55 to 25°C	≤ 85°C	≤ 125°C	
f_{max}	Maximum Clock Frequency (50% Duty Cycle) (Figures 3, 4 and 9)	2.0 4.5 6.0	6.0 30 35	4.8 24 28	4.0 20 24	MHz
t_{PLH}, t_{PHL}	Maximum Propagation Delay, Input A to Output B (or Input B to Output A) (Figures 1, 2 and 9)	2.0 4.5 6.0	170 34 29	215 43 37	255 51 43	ns
t_{PLH}, t_{PHL}	Maximum Propagation Delay, A–to–B Clock to Output B (or B–to–A Clock to Output A) (Figures 3, 4 and 9)	2.0 4.5 6.0	220 44 37	275 55 47	330 66 56	ns
t_{PLH}, t_{PHL}	Maximum Propagation Delay, A–to–B Source to Output B (or B–to–A Source to Output A) (Figures 5, 6 and 9)	2.0 4.5 6.0	170 34 29	215 43 37	255 51 43	ns
t_{PLZ}, t_{PHZ}	Maximum Propagation Delay, Output Enable to Output A or B (Figures 7, 8 and 10)	2.0 4.5 6.0	175 35 30	220 44 37	265 53 45	ns
t_{PZL}, t_{PZH}	Maximum Propagation Delay, Direction or Output Enable to Output A or B (Figures 7, 8 and 10)	2.0 4.5 6.0	175 35 30	220 44 37	265 53 45	ns
t_{TLH}, t_{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 9)	2.0 4.5 6.0	60 12 10	75 15 13	90 18 15	ns
C_{in}	Maximum Input Capacitance	—	10	10	10	pF
C_{out}	Maximum Three–State Output Capacitance (Output in High–Impedance State)	—	15	15	15	pF

NOTES:
1. For propagation delays with loads other than 50 pF, see Chapter 2.
2. Information on typical parametric values can be found in Chapter 2.

		Typical @ 25°C, V_{CC} = 5.0 V	
C_{PD}	Power Dissipation Capacitance (Per Channel)*	60	pF

* Used to determine the no–load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$. For load considerations, see Chapter 2.

TIMING REQUIREMENTS (Input $t_r = t_f$ = 6 ns)

Symbol	Parameter	V_{CC} V	Guaranteed Limit			Unit
			– 55 to 25°C	≤ 85°C	≤ 125°C	
t_{su}	Minimum Setup Time, Input A to A–to–B Clock (or Input B to B–to–A Clock) (Figures 3 and 4)	2.0 4.5 6.0	100 20 17	125 25 21	150 30 26	ns
t_h	Minimum Hold Time, A–to–B Clock to Input A (or B–to–A Clock to Input B) (Figures 3 and 4)	2.0 4.5 6.0	5 5 5	5 5 5	5 5 5	ns
t_w	Minimum Pulse Width, A–to–B Clock (or B–to–A Clock) (Figures 3 and 4)	2.0 4.5 6.0	80 16 14	100 20 17	120 24 20	ns
t_r, t_f	Maximum Input Rise and Fall Times (Figure 1)	2.0 4.5 6.0	1000 500 400	1000 500 400	1000 500 400	ns

NOTE: Information on typical parametric values can be found in Chapter 2.

FUNCTION TABLE — HC646

Control Inputs						Data Port Status		Storage Flip–Flop States		Description of Operation
Output Enable	Direc–tion	A–to–B Clock	B–to–A Clock	A–to–B Source	B–to–A Source	A	B	Q_A	Q_B	
H	X	H, L, ↘	H, L, ↘	X	X	Input: X	Input: X	no change	no change	The output functions of the A and B ports are disabled
		↗	↗	X	X	L H X X	X X L H	L H X X	X X L H	The ports may be used as inputs to the storage flip–flops. Data at the inputs are clocked into the flip–flops *with the rising edge of the Clocks.*
L	H	H, L, ↘	X*	L	X	Input: L H	Output: L H	no change no change	no change no change	The output mode of the B data port is enabled and behaves according to the following logic equation: $B = [A \bullet (\overline{\text{A–to–B Source}})] + [Q_A \bullet (\text{A–to–B Source})]$ 1.) When A–to–B Source is low, the data at the A data port are displayed at the B data port. The states of the storage flip–flops are not affected.
				H	X	X	Q_A	*no change*	*no change*	2.) *When A–to–B Source is high, the* states of the A storage flip–flops are displayed at the B data port.
		↗	X*	L	X	L H	L H	L H	no change no change	3.) When A–to–B Source is low, the data at the A data port are clocked into the A storage flip–flops by a rising–edge signal on the A–to–B Clock.
				H	X	L H	Q_A Q_A	L H	no change no change	4.) When A–to–B Source is high, the data at the A data port are clocked into the A storage flip–flops by a rising–edge signal on the A–to–B Clock. The states, Q_A, of the storage flip–flops propagate directly to the B data port.
L	L	X*	H, L, ↘	X	L	Output: L H	Input: L H	no change no change	no change no change	The output mode of the A data port is enabled and behaves according to the following logic equation: $A = [B \bullet (\overline{\text{B–to–A Source}})] + [Q_B \bullet (\text{B–to–A Source})]$ 1.) When B–to–A Source is low, the data at the B data port are displayed at the A data port. The *states of the storage flip–flops are* not affected.
				X	H	Q_B	X	no change	no change	2.) When B–to–A Source is high, the states of the B storage flip–flops are displayed at the A data port.
		X*	↗	X	L	L H	L H	no change no change	L H	3.) When B–to–A Source is low, the data at the B data port are clocked into the B storage flip–flops by a rising–edge signal on the B–to–A Clock.
				X	H	Q_B Q_B	L H	no change no change	L H	4.) When B–to–A Source is high, the data at the B data port are clocked into the B storage flip–flops by a rising–edge signal on the B–to–A Clock. The states, Q_B, of the storage flip–flops propagate directly to the A data port.

* The clocks are not internally gated with either the Output Enables or the Source inputs. Therefore, data at the A and B ports may be clocked into the storage flip–flops at any time.

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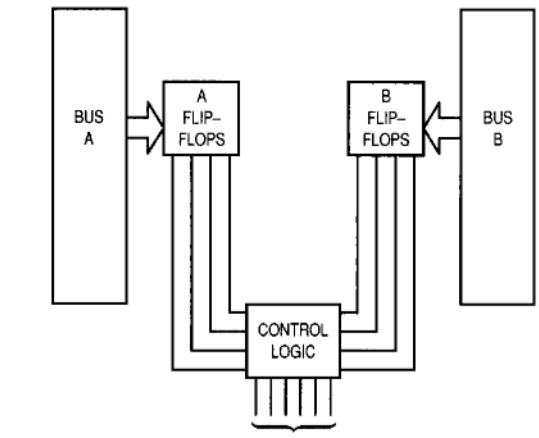
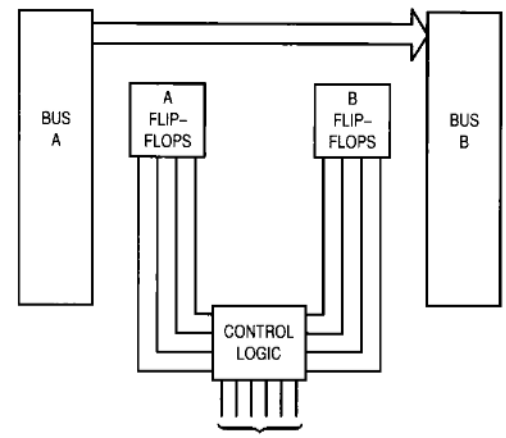
TYPICAL APPLICATIONS



CONTROL PINS	(3) DIRECTION	(21) OUTPUT ENABLE	(1) A–TO–B CLOCK	(23) B–TO–A CLOCK	(2) A–TO–B SOURCE	(22) B–TO–A SOURCE
	X	H	↗	↗	X	X

Data Storage From A and/or B Bus



CONTROL PINS	(3) DIRECTION	(21) OUTPUT ENABLE	(1) A–TO–B CLOCK	(23) B–TO–A CLOCK	(2) A–TO–B SOURCE	(22) B–TO–A SOURCE
	H	L	X	X	L	X

Real–Time Transfer From Bus A to Bus B

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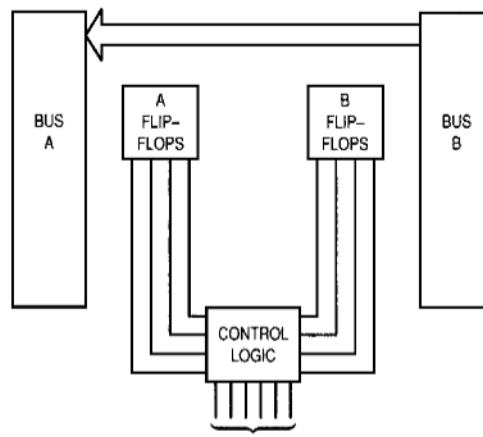


CONTROL PINS	(3) DIRECTION	(21) OUTPUT ENABLE	(1) A–TO–B CLOCK	(23) B–TO–A CLOCK	(2) A–TO–B SOURCE	(22) B–TO–A SOURCE
	L	L	X	X	X	L

Real–Time Transfer From Bus B to Bus A

TIMING DIAGRAMS AND SWITCHING DIAGRAMS — HC646

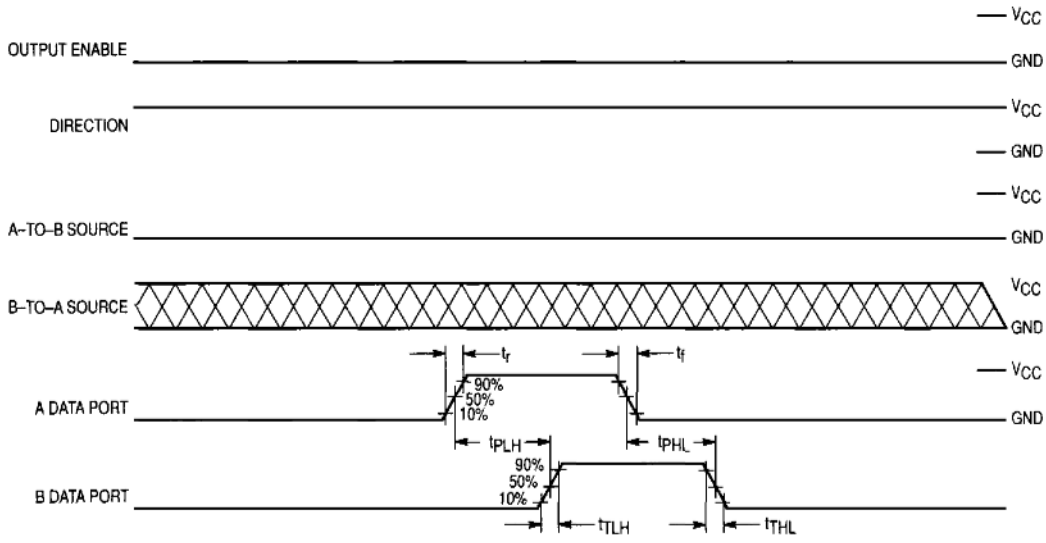


Figure 1. A Data Port = Input, B Data Port = Output

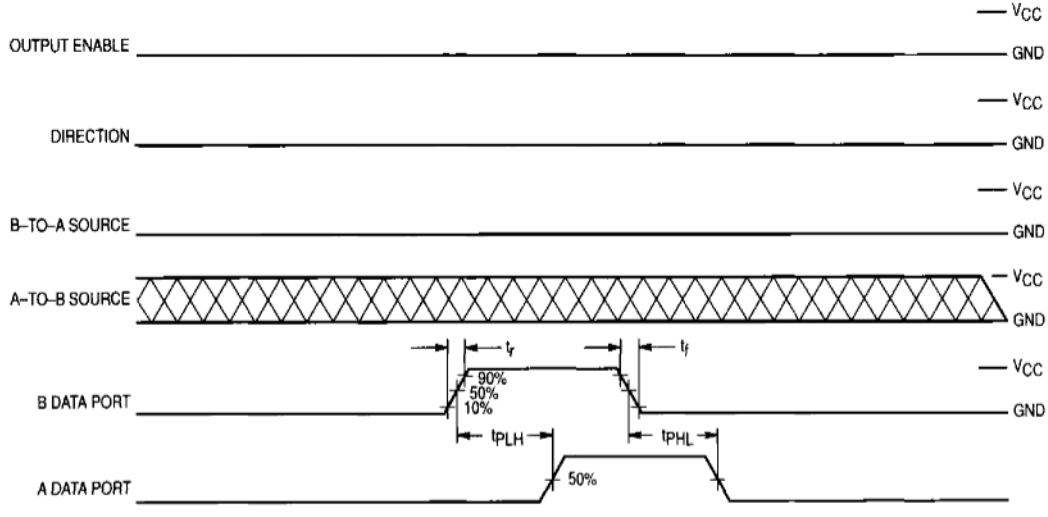
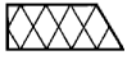


Figure 2. A Data Port = Output, B Data Port = Input

NOTE:  = Don't Care State

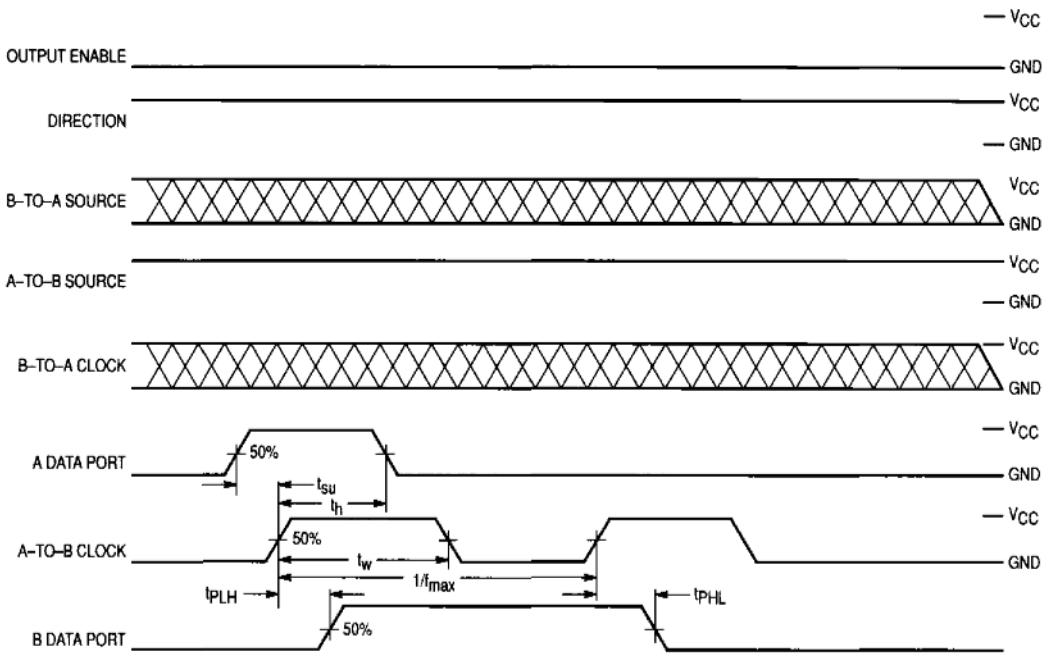


Figure 3. A Data Port = Input, B Data Port = Output

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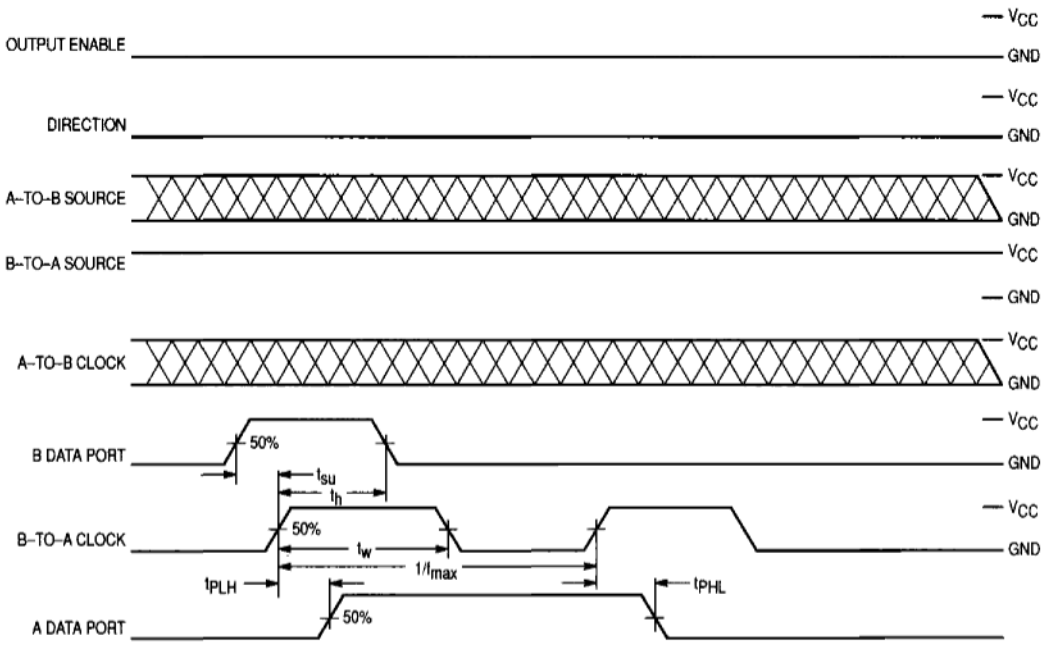
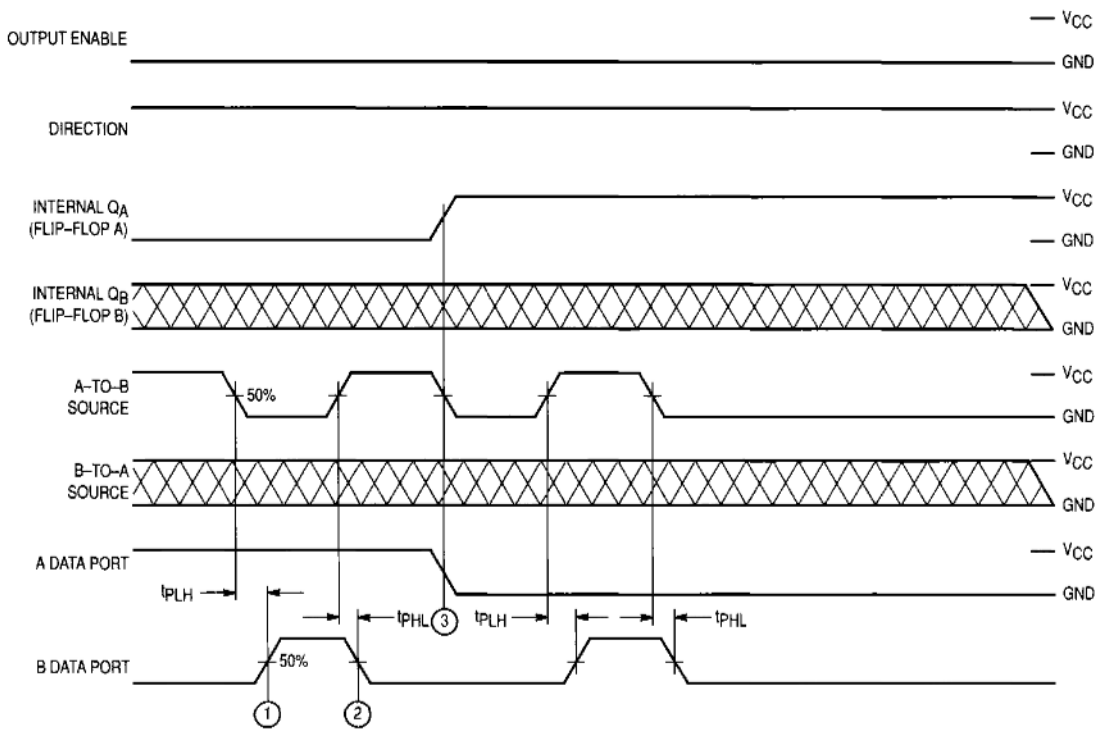
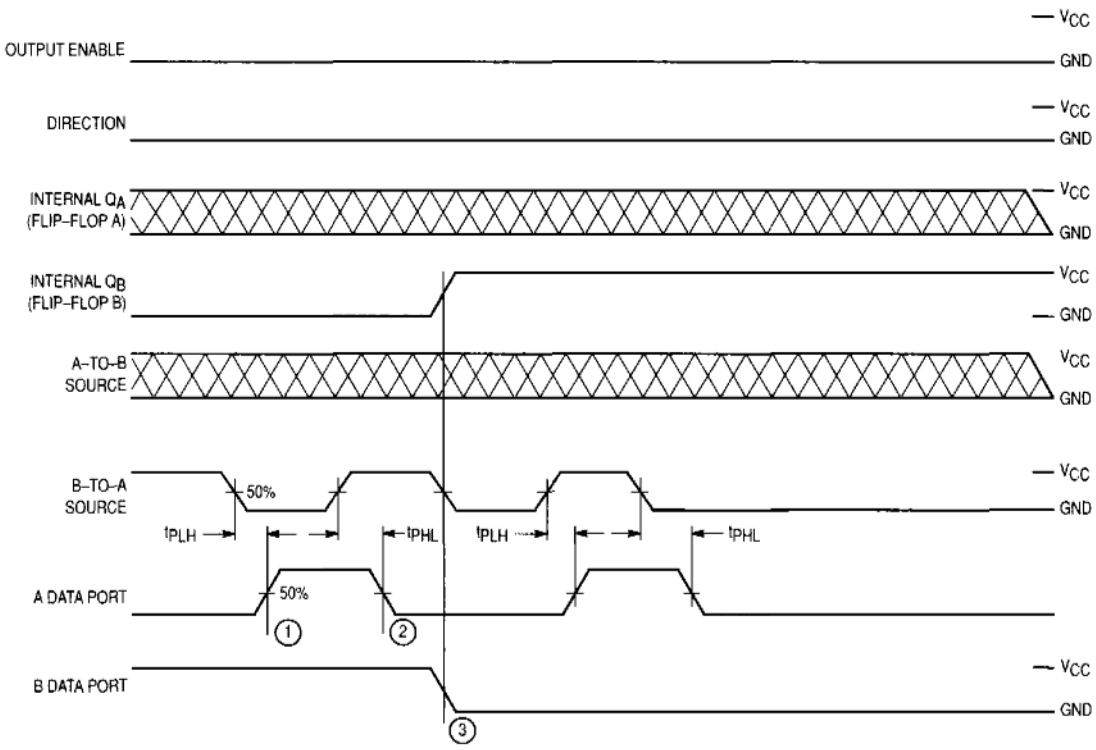


Figure 4. B Data Port = Input, A Data Port = Output



NOTES:
1. B Data Port (output) changes from the level of the storage flip–flop, Q_A, to the level of A Data Port (input).
2. B Data Port (output) changes from the level of the A Data Port (input) to the level of the storage flip–flop, Q_A.
3. The A storage flip–flop, A–to–B Source, and A Data Port (input) have simultaneously changed states.

Figure 5. A Data Port = Input, B Data Port = Output



NOTES:
1. A Data Port (output) changes from the level of the storage flip–flop, Q_B, to the level of B Data Port (input).
2. A Data Port (output) changes from the level of the B Data Port (input) to the level of the storage flip–flop, Q_B.
3. The B storage flip–flop, B–to–A Source, and B Data Port (input) have simultaneously changed states for the purpose of this example. A Data Port (output) is now displaying the voltage level of B Data Port (input).

Figure 6. A Data Port = Output, B Data Port = Input

PIN DESCRIPTIONS

INPUTS/OUTPUTS

A0–A7 (Pins 4–11) and B0–B7 (Pins 20–13)

A and B data ports. These pins may function either as inputs to or outputs from the transceivers.

CONTROL INPUTS

Output Enable (Pin 21)

Active–low output enable. When this pin is low, the outputs are enabled and function normally. When this pin is high, the A and B data ports are in high–impedance states. See the Function Table.

Direction (Pin 3)

Data direction control. When the Output Enable pin is low, this control pin determines the direction of data flow. When Direction is high, the A data ports are inputs and the B data ports are outputs. When Direction is low, the A data ports are outputs and the B data ports are inputs.

A–to–B Clock, B–to–A Clock (Pins 1, 23)

Clocks for the internal D flip–flops. With a low–to–high transition on the appropriate Clock pin, data on the A (or B) inputs are clocked into the internal A (or B) flip–flops. These clocks are not internally gated with the Output Enable or the Direction pins, therefore data at the A and B pins may be clocked into the storage flip–flops at any time.

A–to–B Source, B–to–A Source (Pins 2, 22)

Data–source selection pins. Depending upon the states of these pins (see the Function Table), data at the outputs may come either from the inputs or from the D flip–flops.

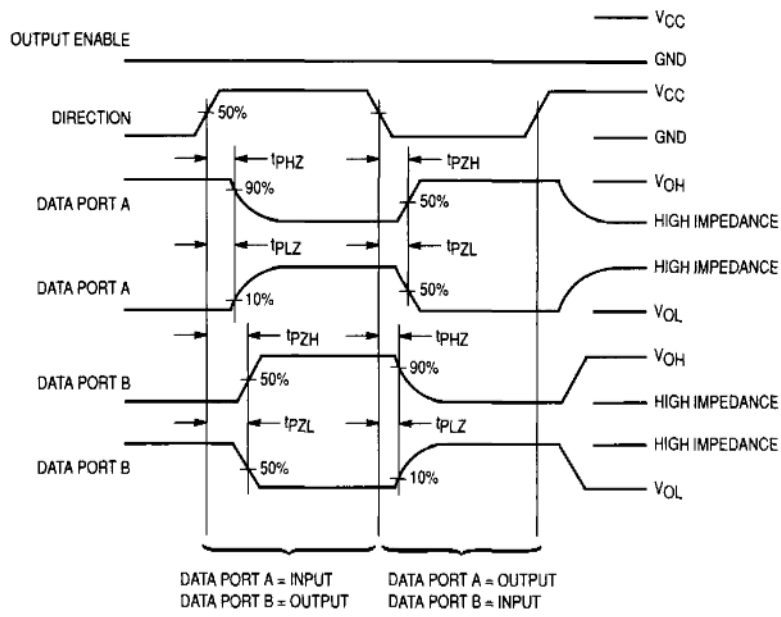


Figure 7.

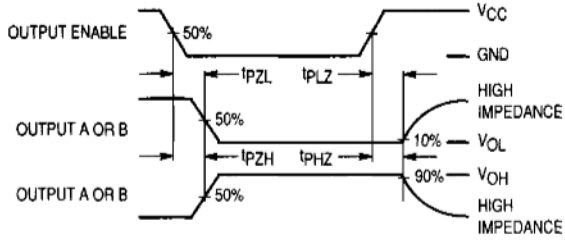
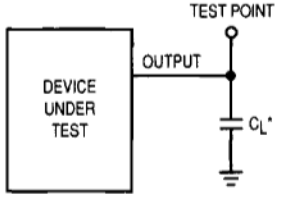
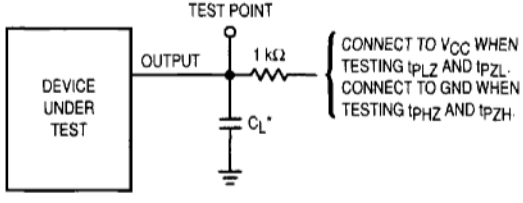


Figure 8.



* Includes all probe and jig capacitance

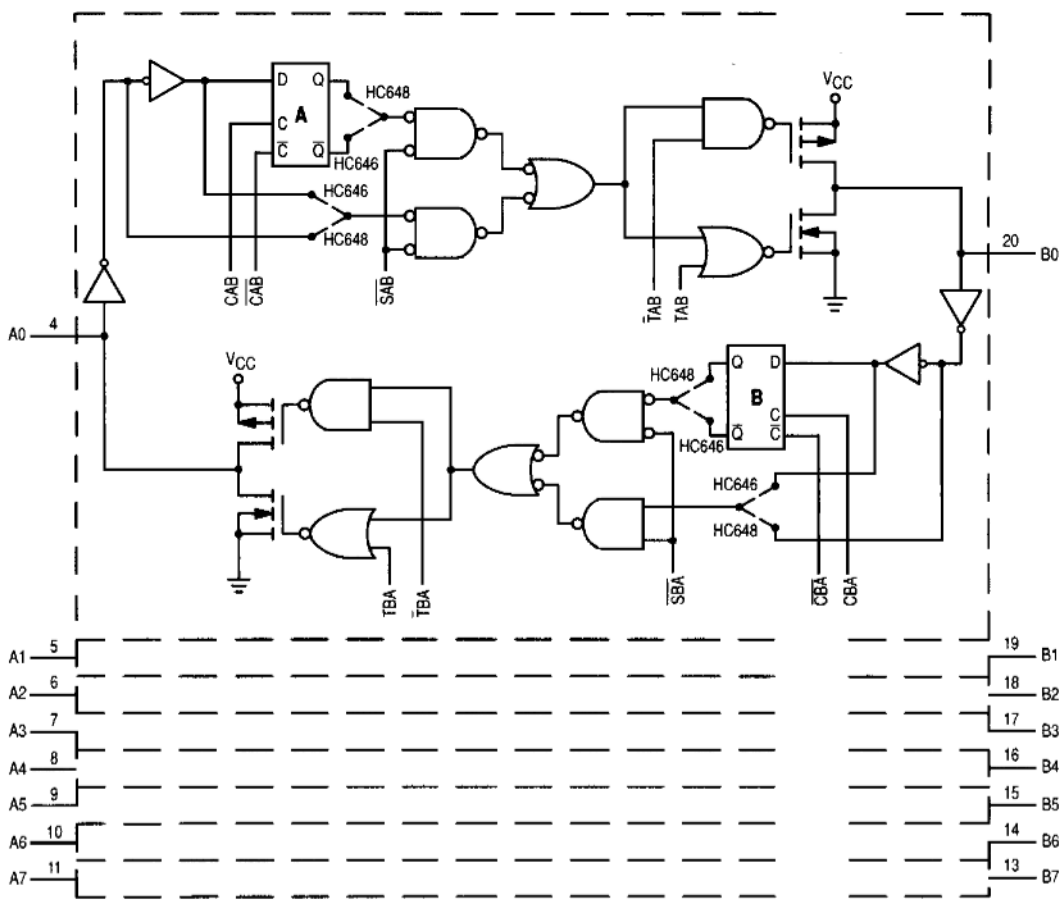
Figure 9. Test Circuit

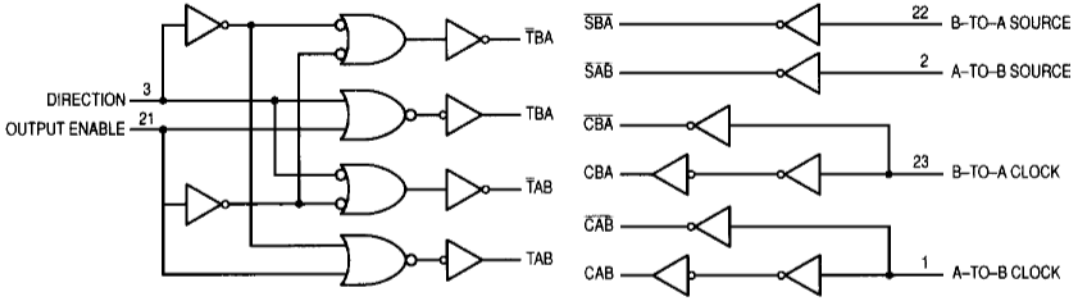


* Includes all probe and jig capacitance

Figure 10. Test Circuit

LOGIC DETAIL





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